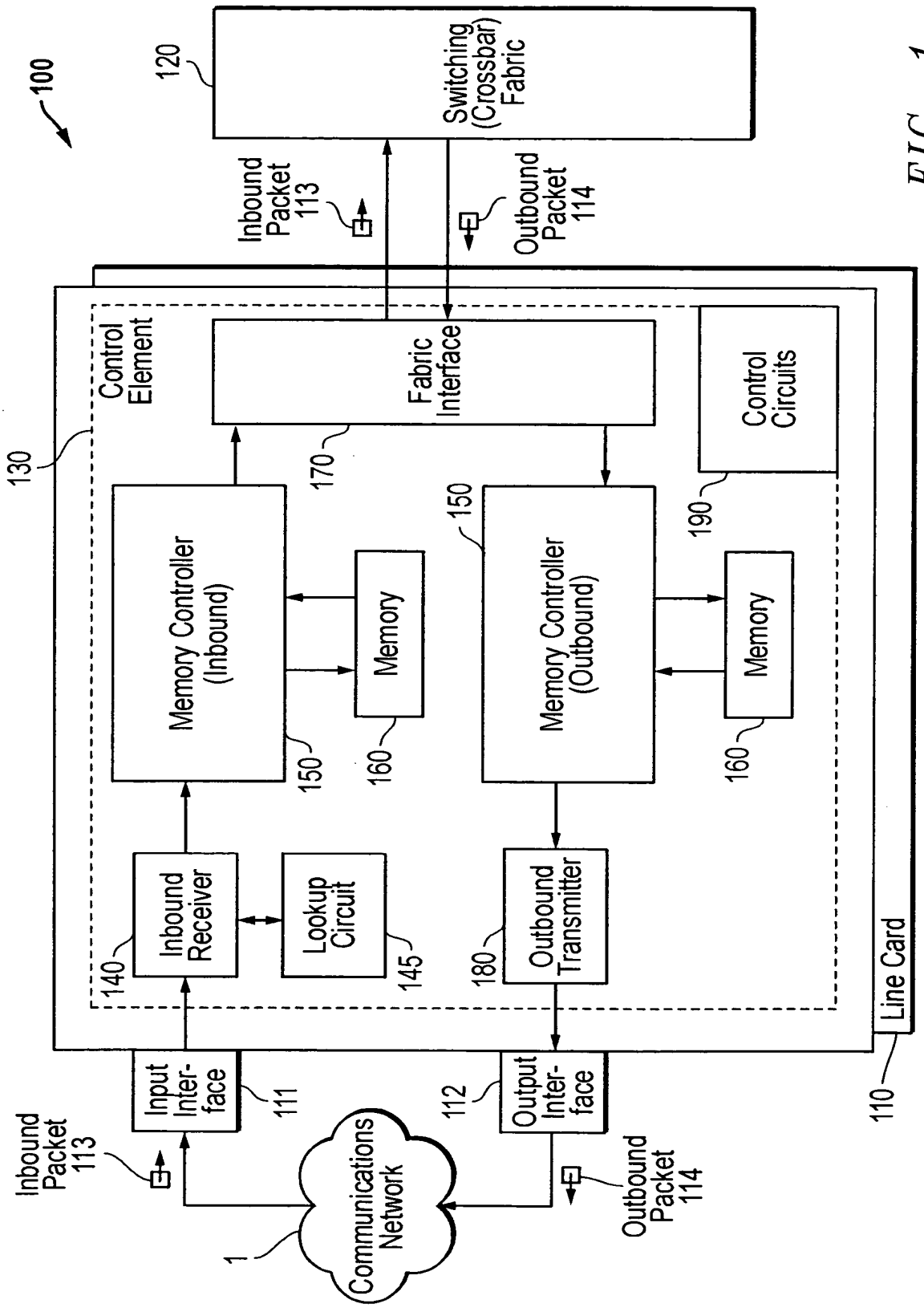

100
120
Switching (Crossbar) Fabric
Inbound Packet 113
Outbound Packet 114
Control Element
130
Fabric Interface
170
Control Circuits
190
Memory Controller (Inbound)
150
Memory
160
Memory Controller (Outbound)
150
Memory
160
Inbound Receiver
140
Lookup Circuit
145
Outbound Transmitter
180
Line Card
110
Input Inter-face
111
Output Inter-face
112
Inbound Packet 113
Communications Network
1
Outbound Packet 114

FIG. 1

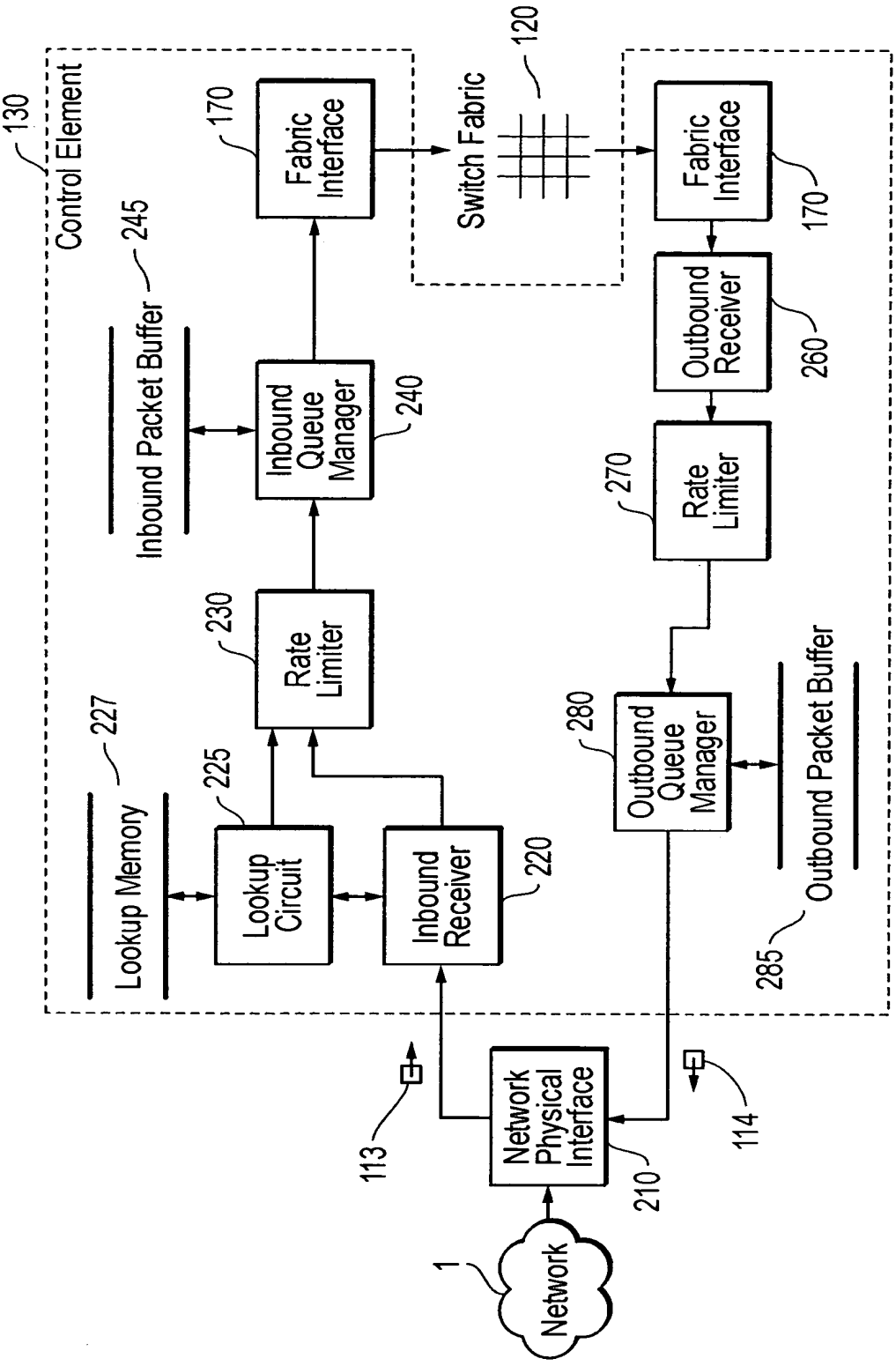

Network
1
Network Physical Interface
210
113
114
Control Element
130
Lookup Memory
227
Lookup Circuit
225
Inbound Receiver
220
Rate Limiter
230
Inbound Packet Buffer
245
Inbound Queue Manager
240
Fabric Interface
170
Switch Fabric
120
Fabric Interface
170
Outbound Receiver
260
Rate Limiter
270
Outbound Queue Manager
280
Outbound Packet Buffer
285

FIG. 2

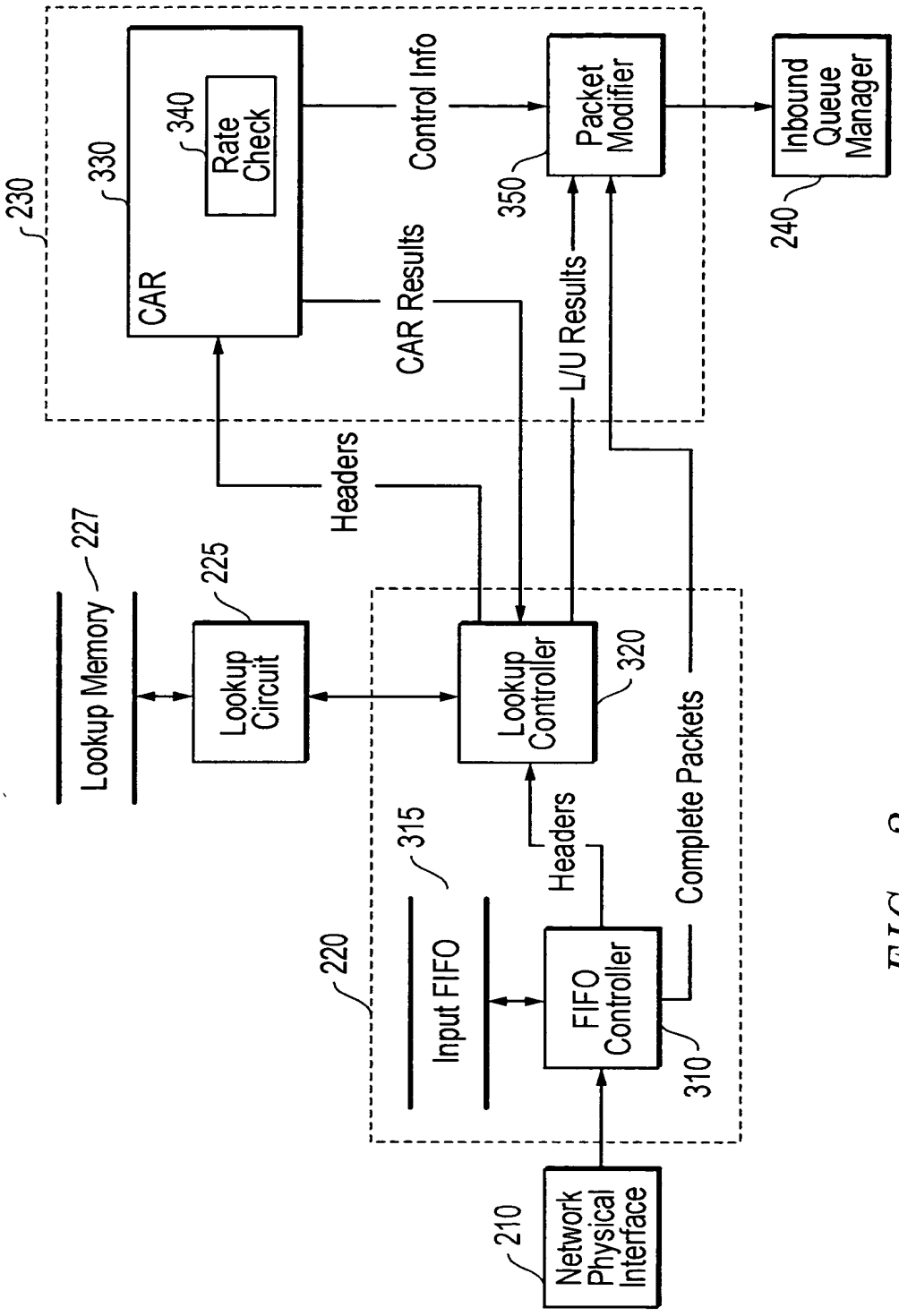

230
330
340
Rate Check
CAR
Control Info
Packet Modifier
350
Inbound Queue Manager
240
CAR Results
L/U Results
Headers
227
Lookup Memory
225
Lookup Circuit
Lookup Controller
320
315
Input FIFO
Headers
Complete Packets
220
FIFO Controller
310
210
Network Physical Interface

FIG. 3

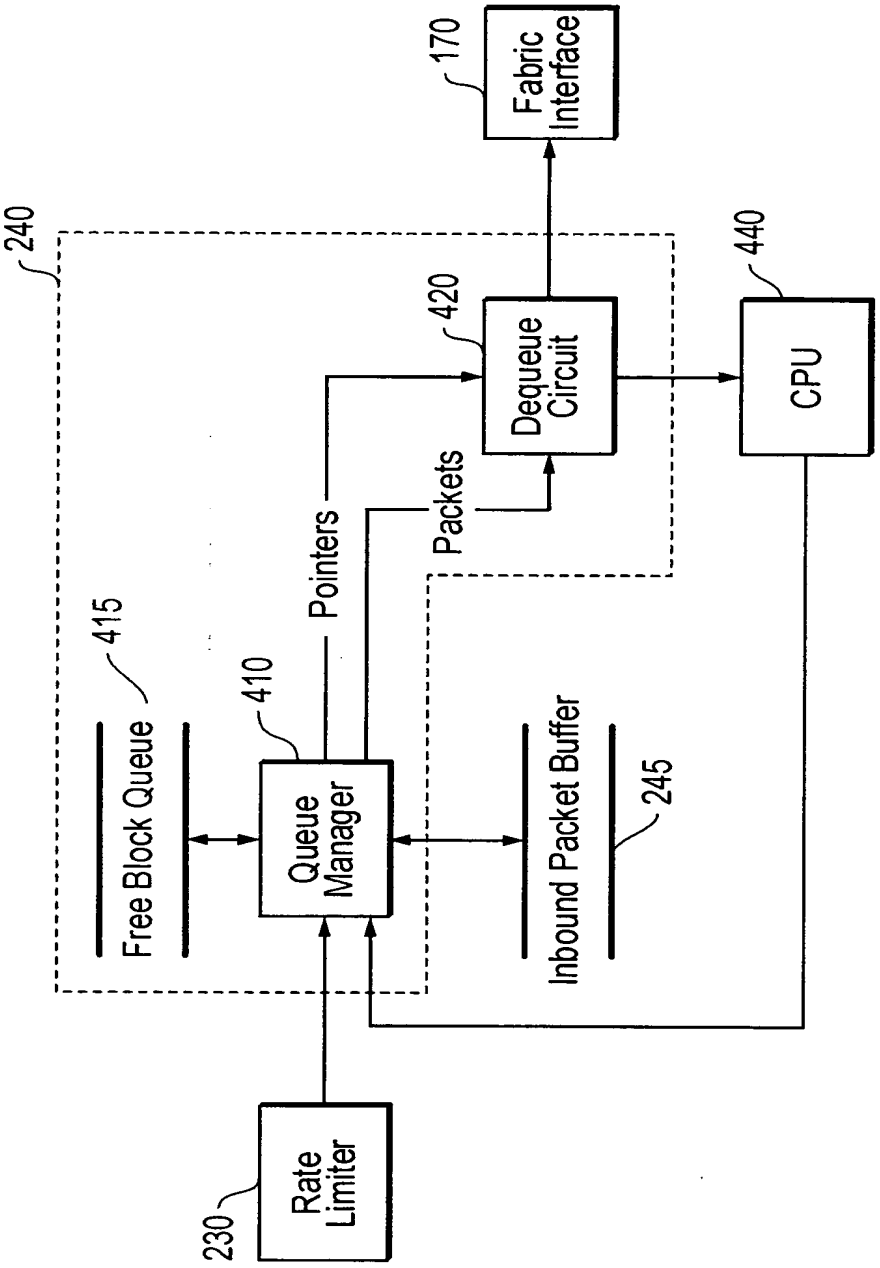

170
Fabric Interface
240
420
Dequeue Circuit
440
CPU
Packets
Pointers
415
Free Block Queue
410
Queue Manager
Inbound Packet Buffer
245
230
Rate Limiter

FIG. 4

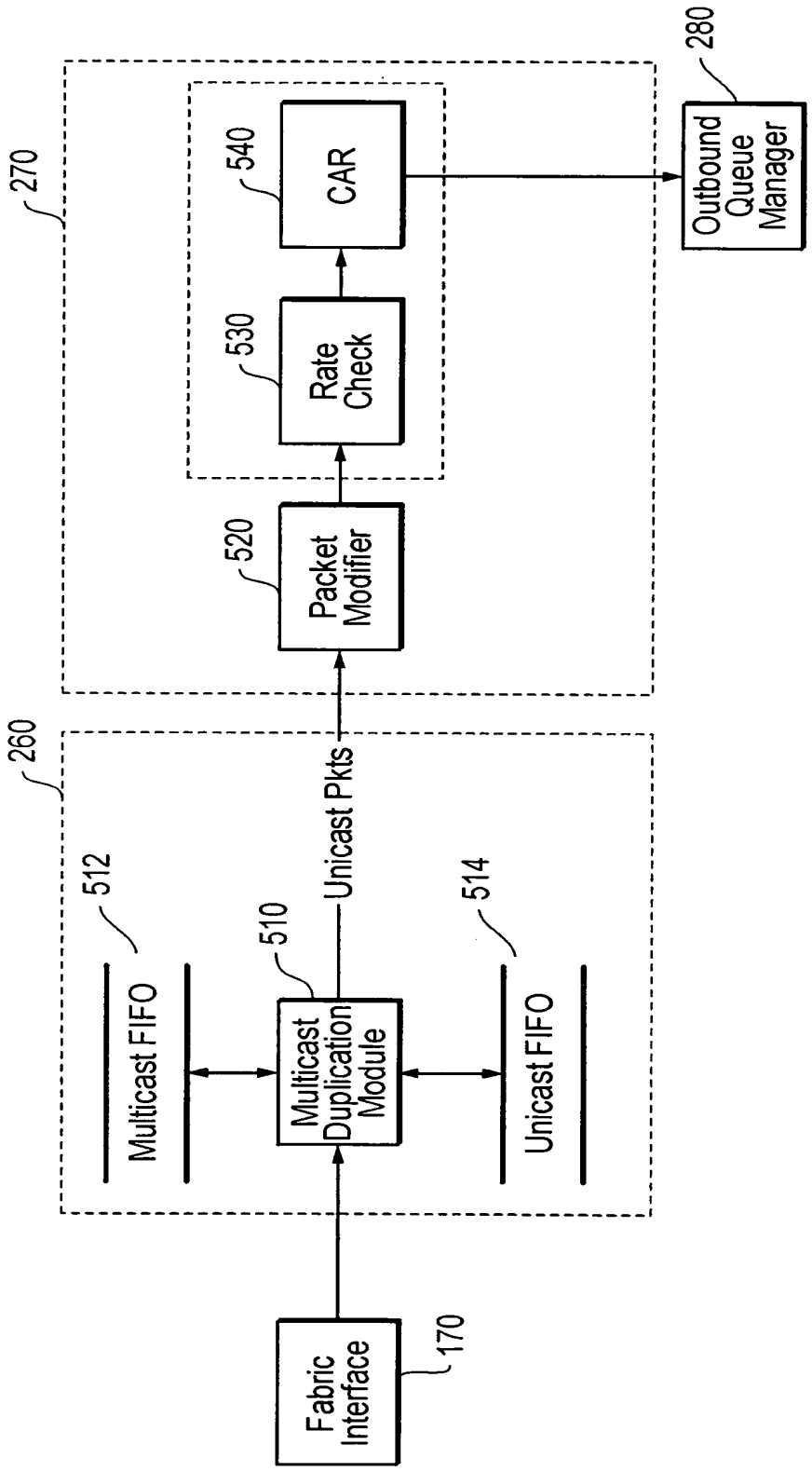

280
Outbound Queue Manager
270
540
CAR
530
Rate Check
520
Packet Modifier
260
512
Multicast FIFO
510
Multicast Duplication Module
Unicast Pkts
514
Unicast FIFO
Fabric Interface
170

FIG. 5

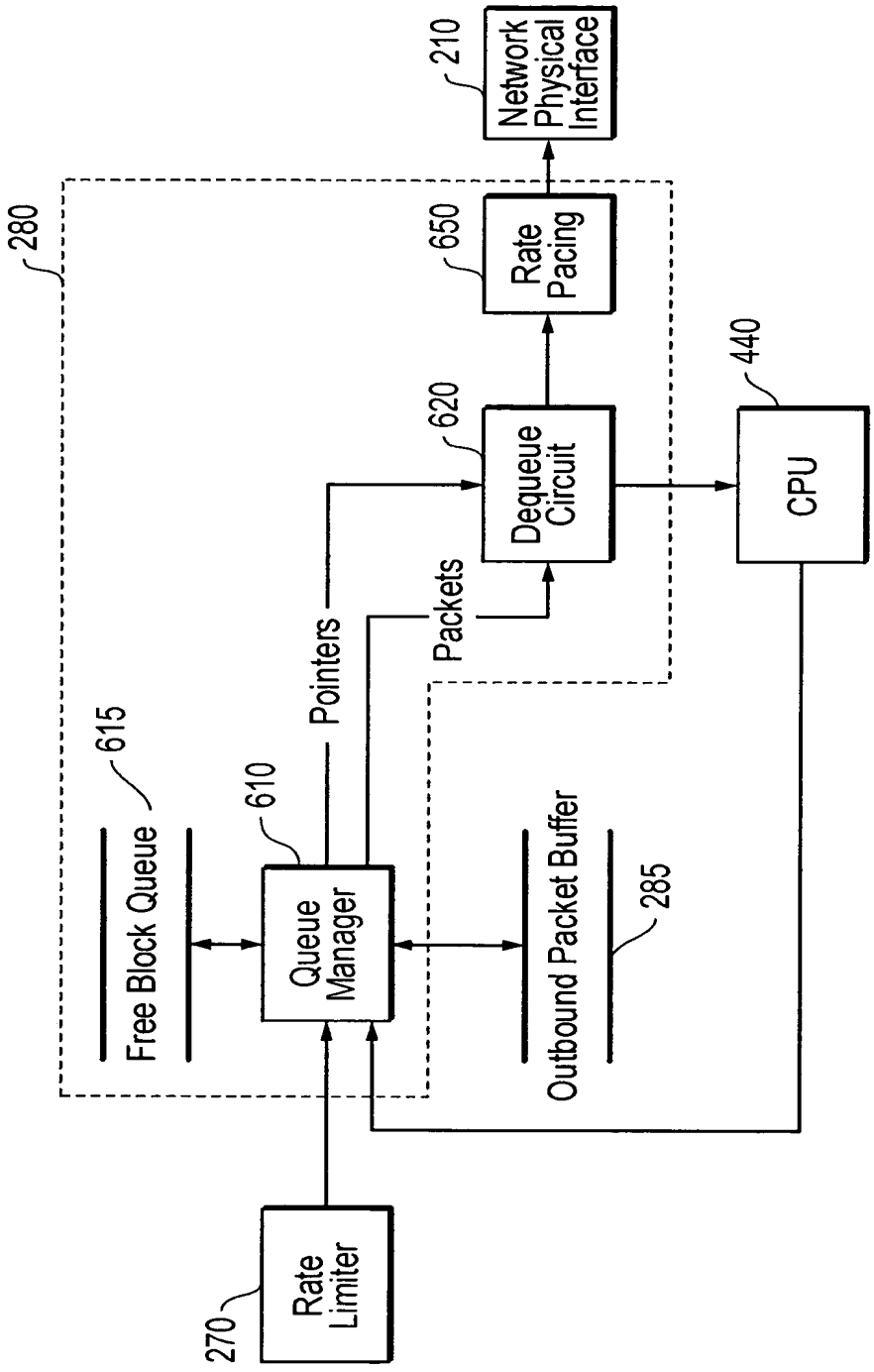

280
210
Network Physical Interface
650
Rate Pacing
620
Dequeue Circuit
440
CPU
Packets
Pointers
615
Free Block Queue
610
Queue Manager
Outbound Packet Buffer
285
270
Rate Limiter

FIG. 6

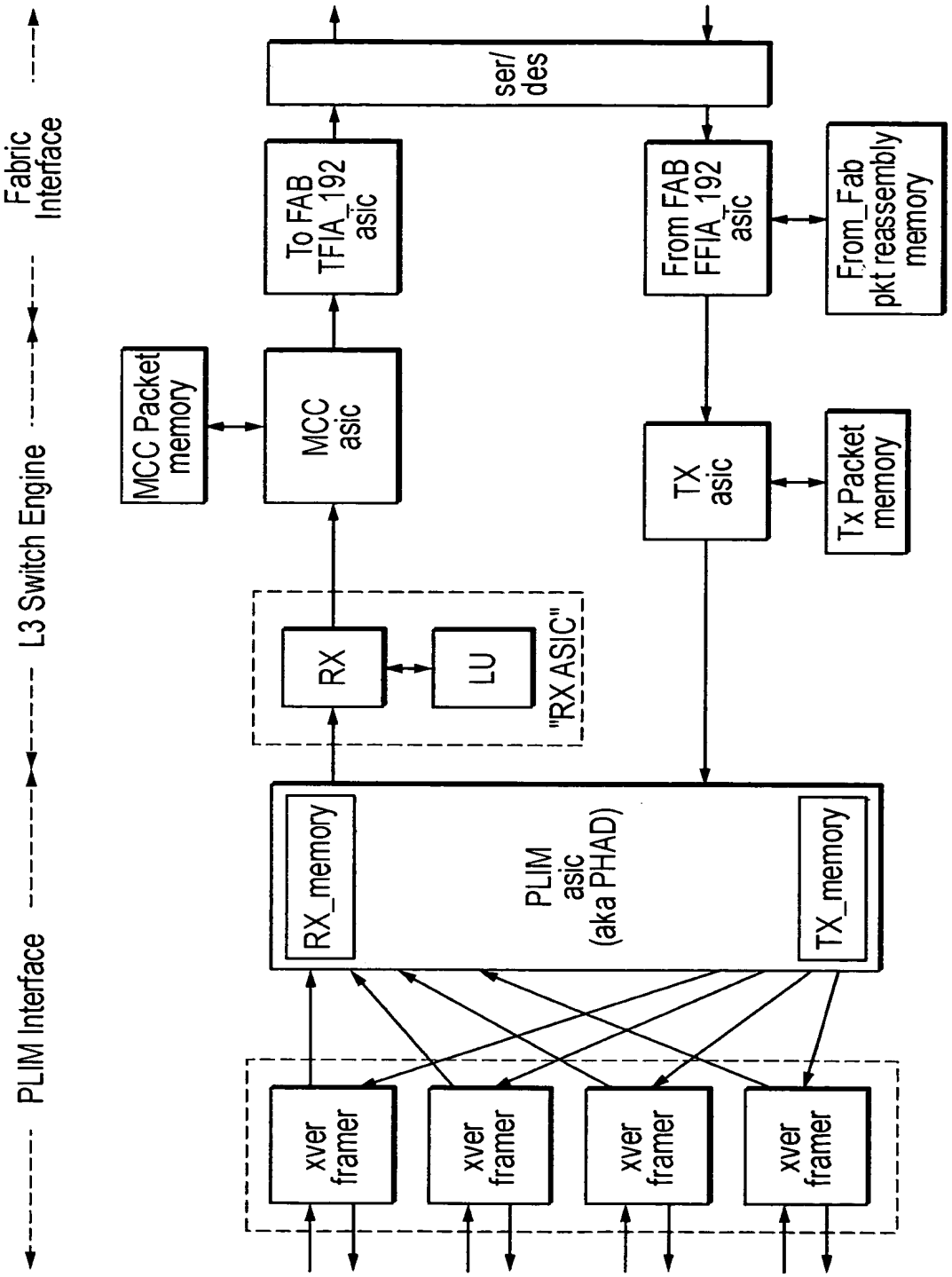

Fabric Interface
L3 Switch Engine
PLIM Interface
ser/ des
To FAB TFIA_192 asic
From FAB FFIA_192 asic
From_Fab pkt reassembly memory
MCC Packet memory
MCC asic
TX asic
Tx Packet memory
RX
LU
"RX ASIC"
RX_memory
PLIM asic (aka PHAD)
TX_memory
xver framer
xver framer
xver framer
xver framer

FIG. 7

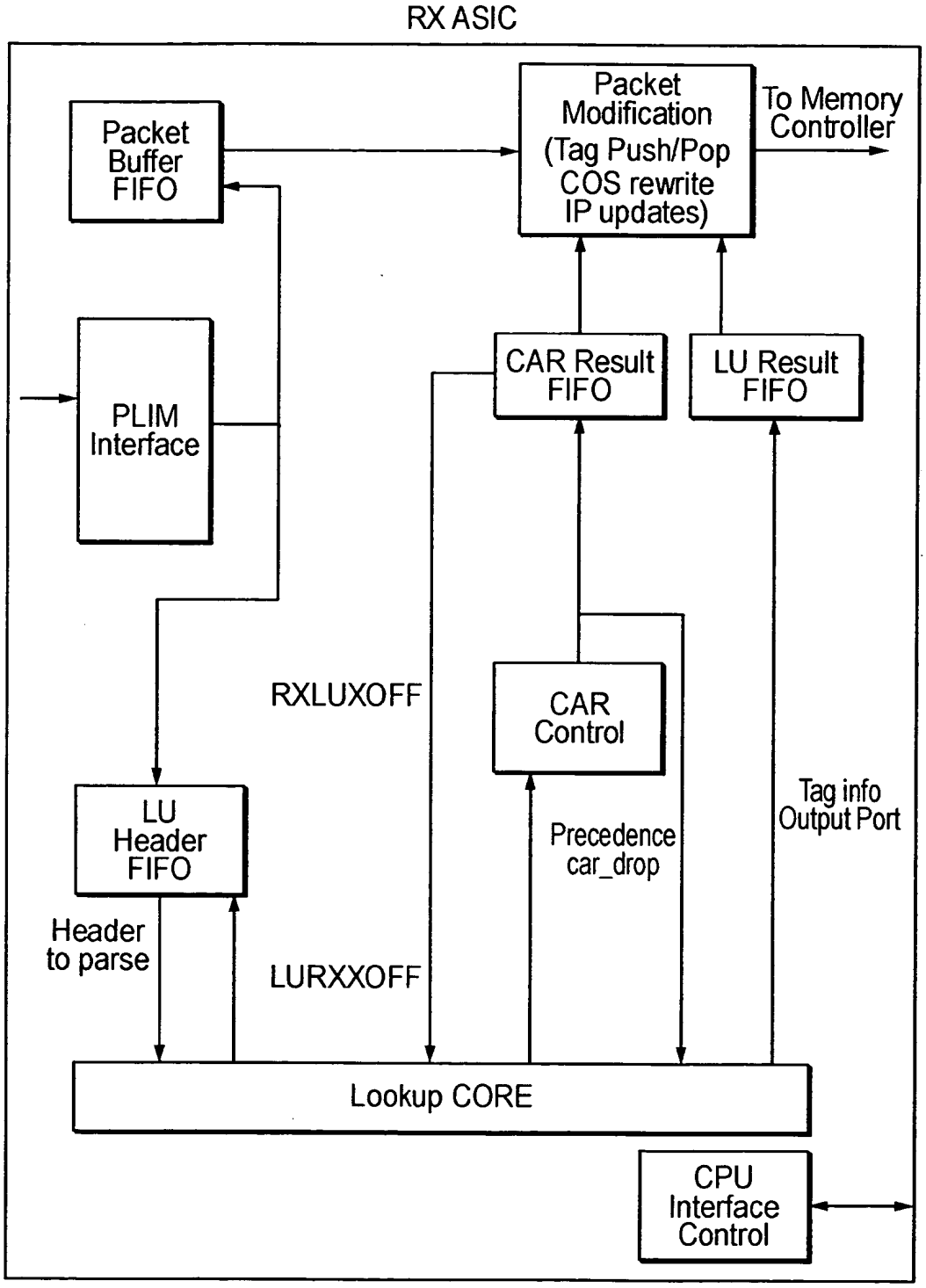

RX ASIC
Packet Buffer FIFO
Packet Modification (Tag Push/Pop COS rewrite IP updates)
To Memory Controller
PLIM Interface
CAR Result FIFO
LU Result FIFO
RXLUXOFF
CAR Control
LU Header FIFO
Tag info Output Port
Precedence car_drop
Header to parse
LURXXOFF
Lookup CORE
CPU Interface Control

FIG. 8

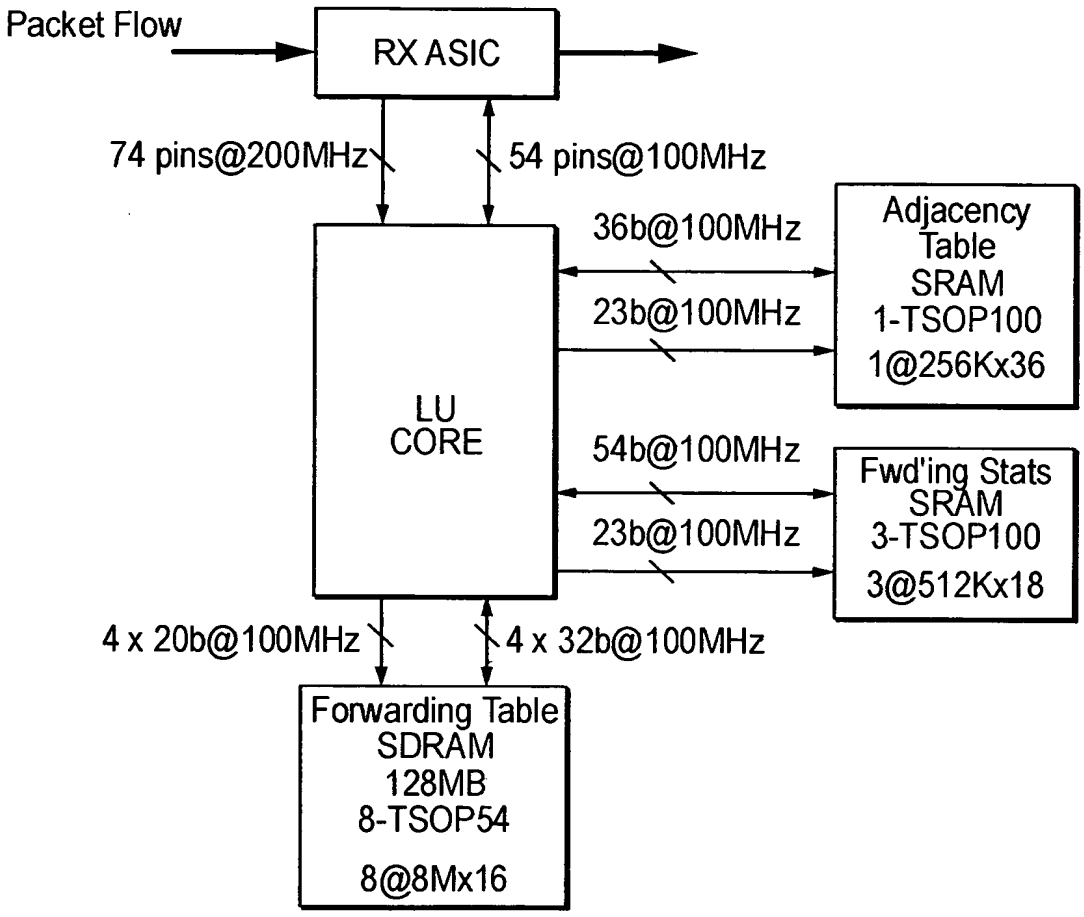

Packet Flow
RX ASIC
74 pins@200MHz
54 pins@100MHz
36b@100MHz
23b@100MHz
Adjacency Table SRAM 1-TSOP100 1@256Kx36
LU CORE
54b@100MHz
23b@100MHz
Fwd'ing Stats SRAM 3-TSOP100 3@512Kx18
4 x 20b@100MHz
4 x 32b@100MHz
Forwarding Table SDRAM 128MB 8-TSOP54 8@8Mx16

FIG. 9

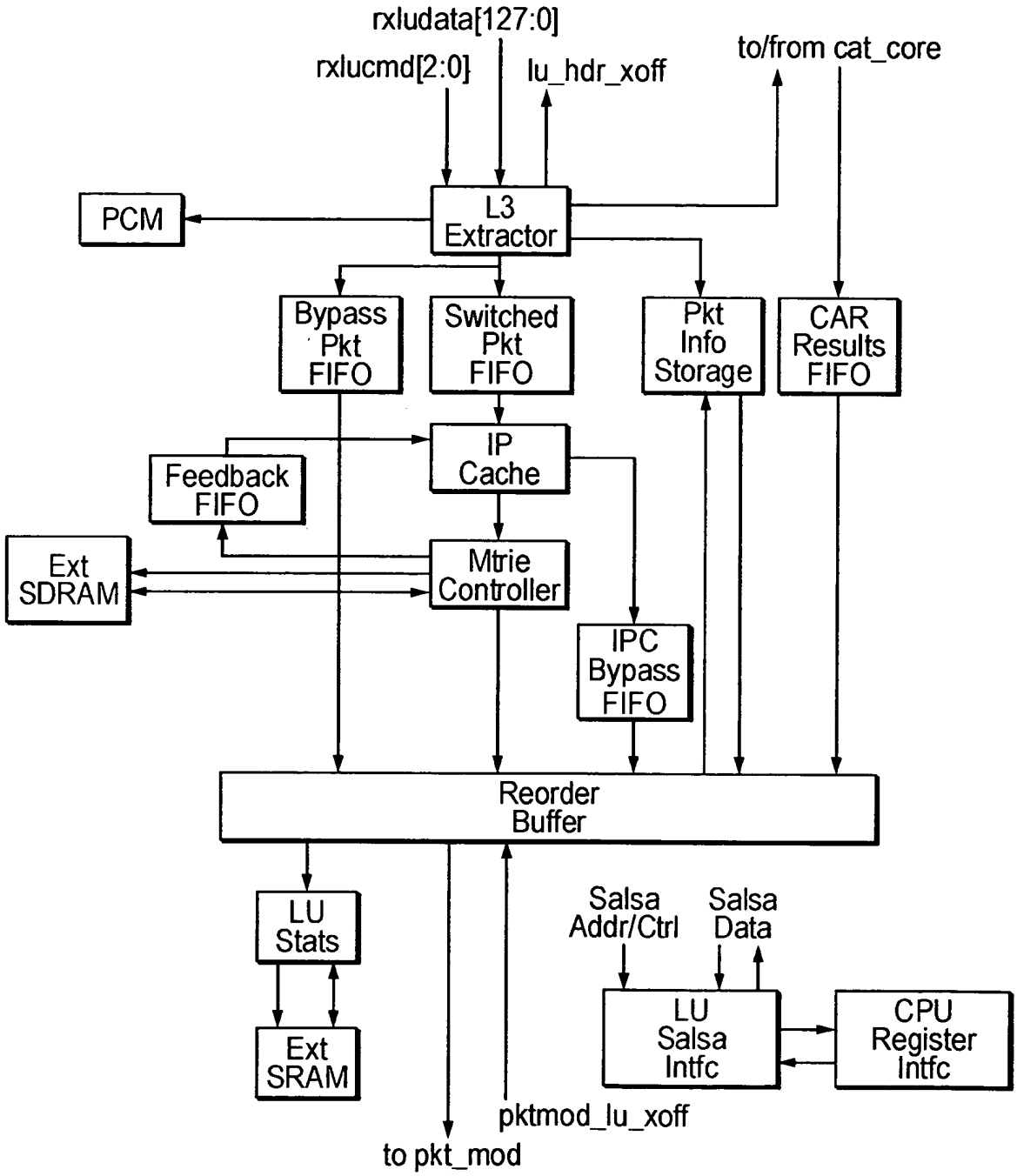

rxludata[127:0]
rxlucmd[2:0]
lu_hdr_xoff
to/from cat_core
PCM
L3 Extractor
Bypass Pkt FIFO
Switched Pkt FIFO
Pkt Info Storage
CAR Results FIFO
IP Cache
Feedback FIFO
Ext SDRAM
Mtrie Controller
IPC Bypass FIFO
Reorder Buffer
LU Stats
Ext SRAM
Salsa Addr/Ctrl
Salsa Data
LU Salsa Intfc
CPU Register Intfc
pktmod_lu_xoff
to pkt_mod

FIG. 10

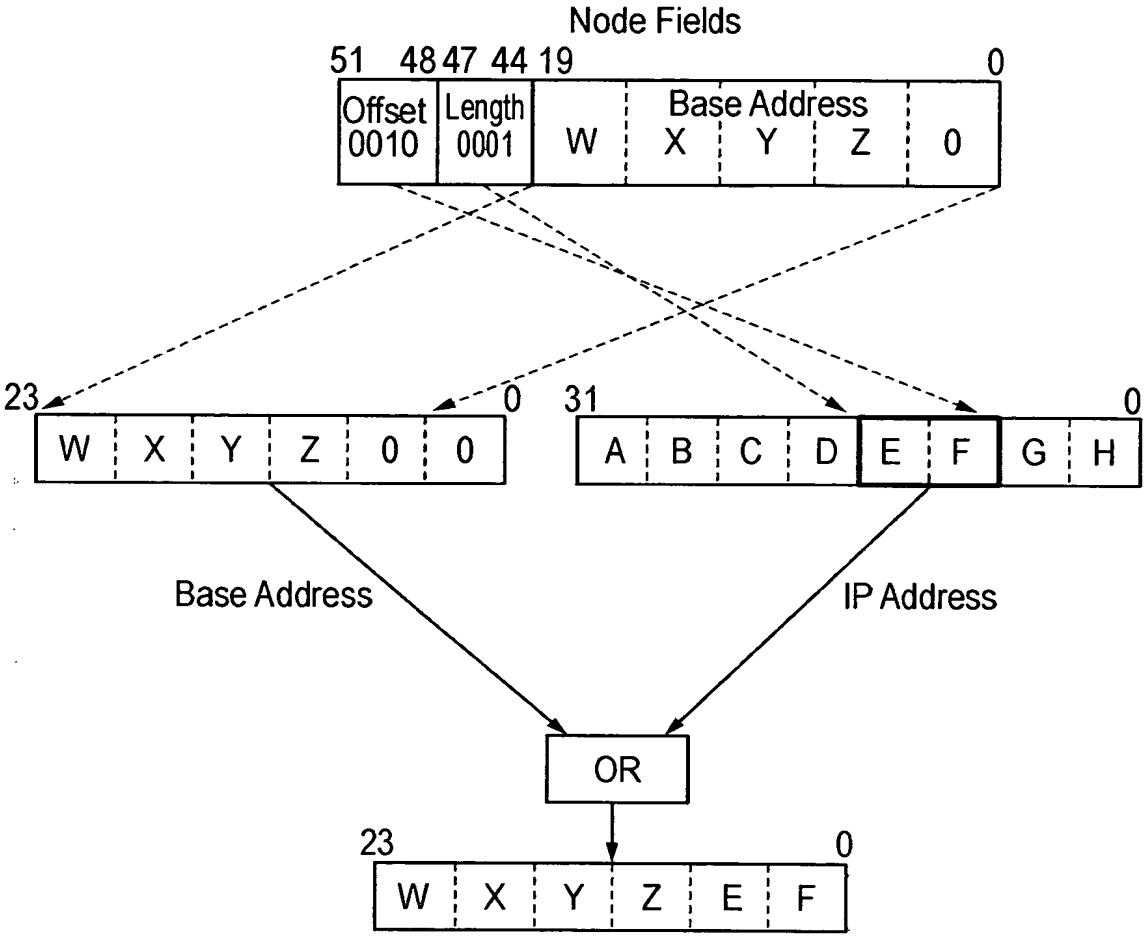

Node Fields
51
48 47
44 19
0
Offset 0010
Length 0001
W
Base Address
X
Y
Z
0
23
0
W
X
Y
Z
0
0
31
0
A
B
C
D
E
F
G
H
Base Address
IP Address
OR
23
0
W
X
Y
Z
E
F

FIG. 11

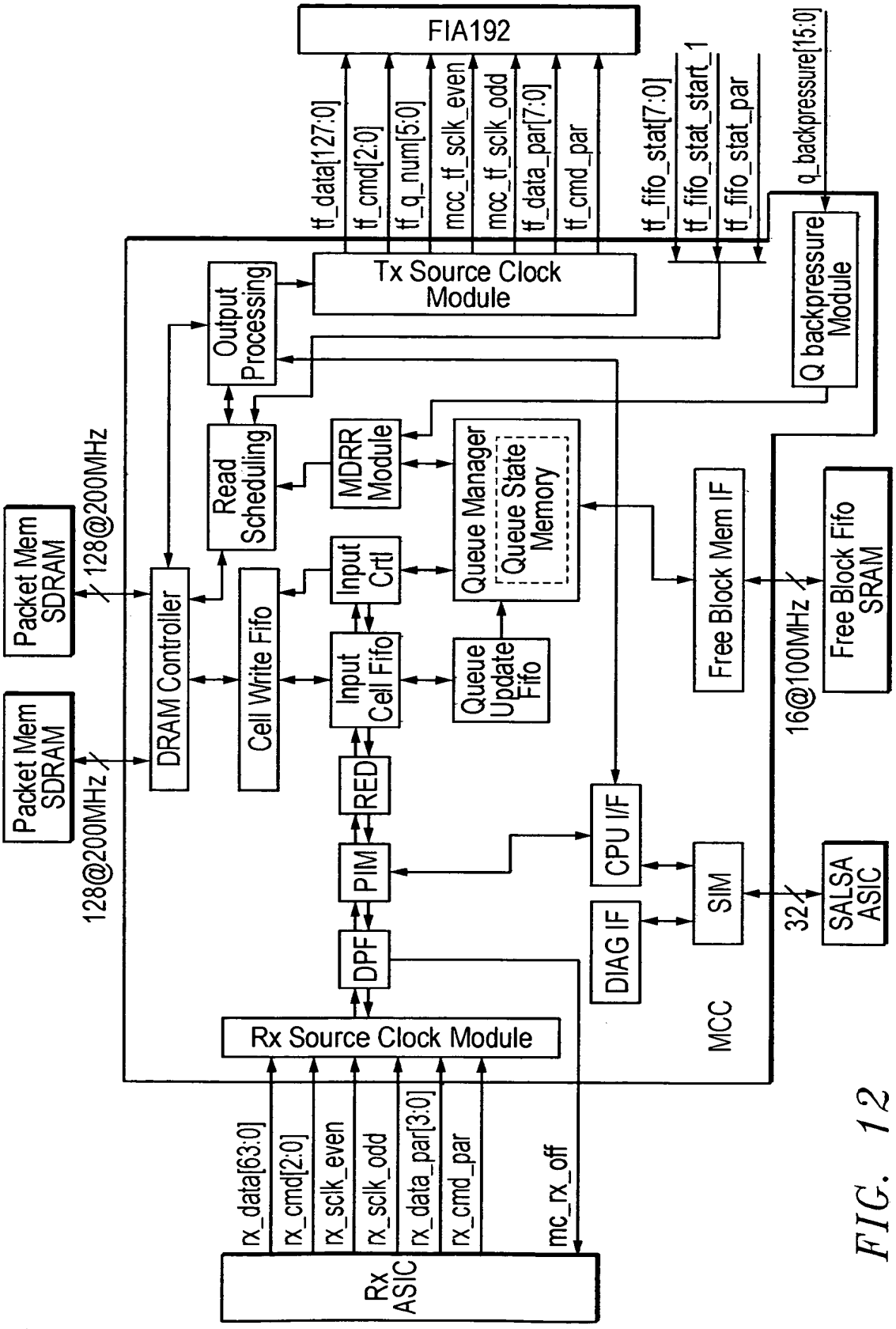
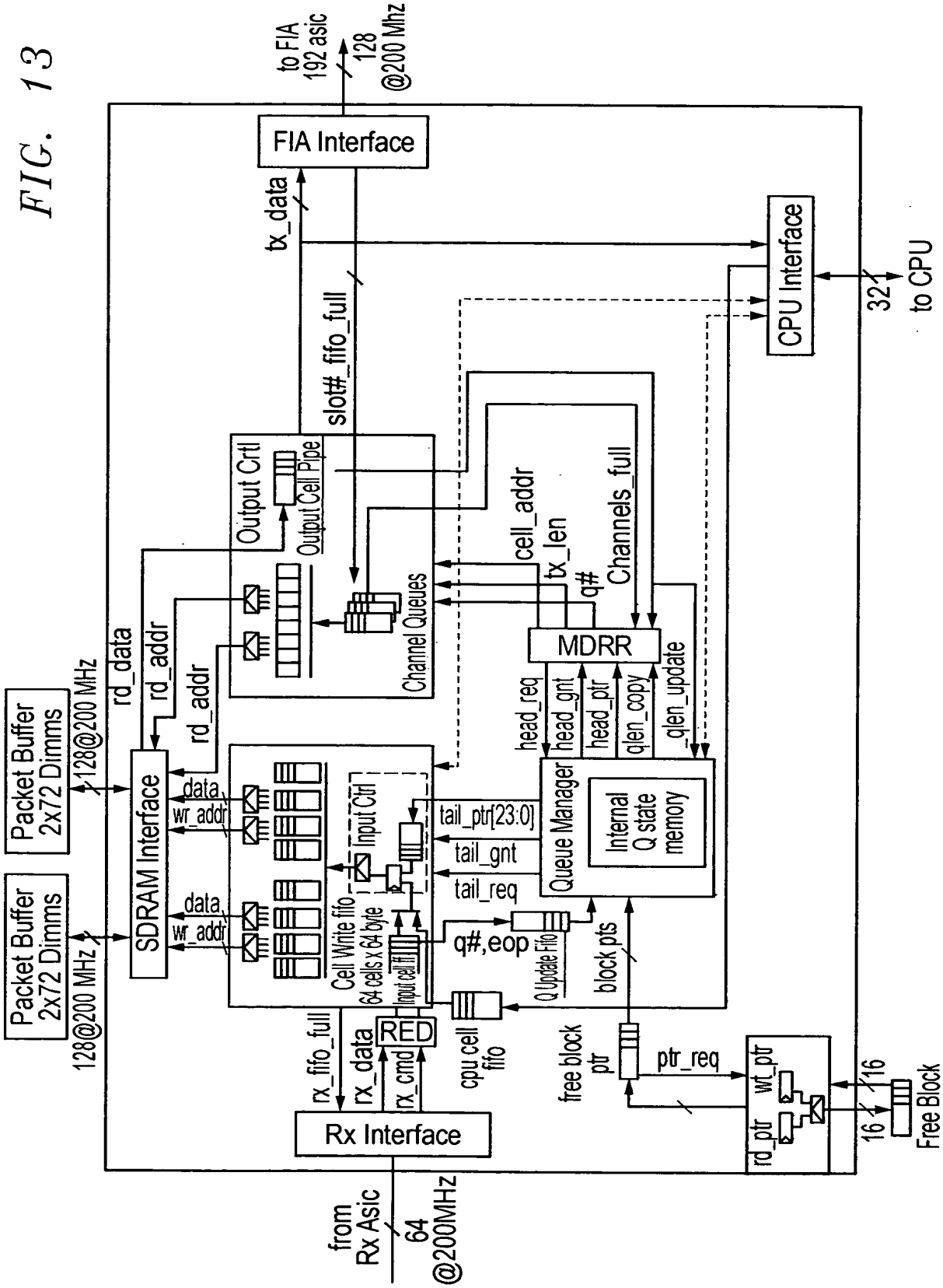

FIA192
tf_data[127:0]
tf_cmd[2:0]
tf_q_num[5:0]
mcc_tf_sclk_even
mcc_tf_sclk_odd
tf_data_par[7:0]
tf_cmd_par
tf_fifo_stat[7:0]
tf_fifo_stat_start_1
tf_fifo_stat_par
q_backpressure[15:0]
Tx Source Clock Module
Output Processing
Q backpressure Module
Read Scheduling
MDRR Module
Queue Manager
Queue State Memory
Input Crtl
Queue Update Fifo
Free Block Mem IF
Free Block Fifo SRAM
16@100MHz
Packet Mem SDRAM
128@200MHz
DRAM Controller
Cell Write Fifo
Input Cell Fifo
RED
PIM
DPF
CPU I/F
DIAG IF
SIM
SALSA ASIC
32
MCC
Rx Source Clock Module
rx_data[63:0]
rx_cmd[2:0]
rx_sclk_even
rx_sclk_odd
rx_data_par[3:0]
rx_cmd_par
mc_rx_off
Rx ASIC

FIG. 12

FIG. 13


to FIA 192 asic
128 @200 Mhz
FIA Interface
tx_data
slot#_fifo_full
CPU Interface
32
to CPU
Output Crtl
Output Cell Pipe
Channel Queues
cell_addr
tx_len
q#
Channels_full
MDRR
head_req
head_gnt
head_ptr
qlen_copy
qlen_update
rd_data
rd_addr
rd_addr
Packet Buffer 2x72 Dimms
128@200 MHz
SDRAM Interface
data
wr_addr
data
wr_addr
Input Ctrl
tail_ptr[23:0]
tail_gnt
tail_req
Queue Manager
Internal Q state memory
Cell Write fifo
64 cells x 64 byte
Input cell fifo
q#,eop
Q Update Fifo
block pts
Packet Buffer 2x72 Dimms
128@200 MHz
rx_fifo_full
rx_data
rx_cmd
RED
cpu cell fifo
free block ptr
ptr_req
rd_ptr
wt_ptr
16
16
Free Block
Rx Interface
from Rx Asic
64
@200MHz

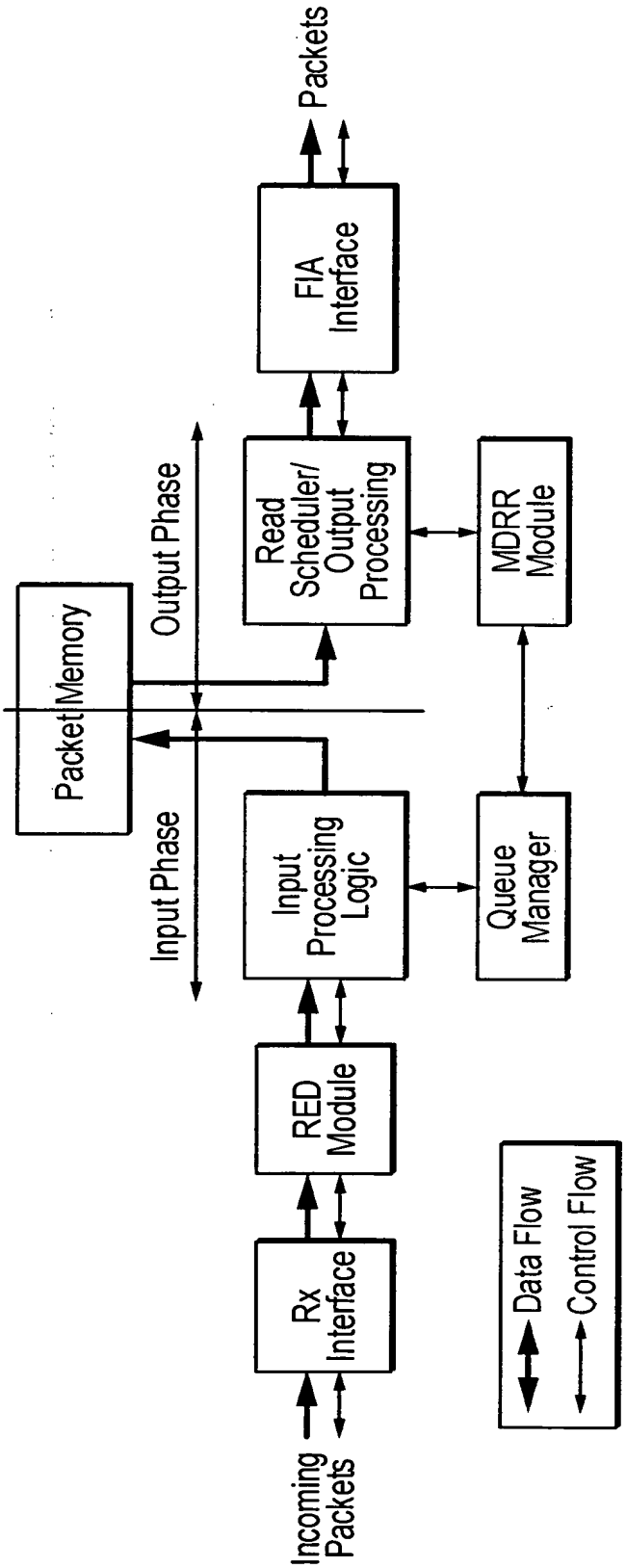
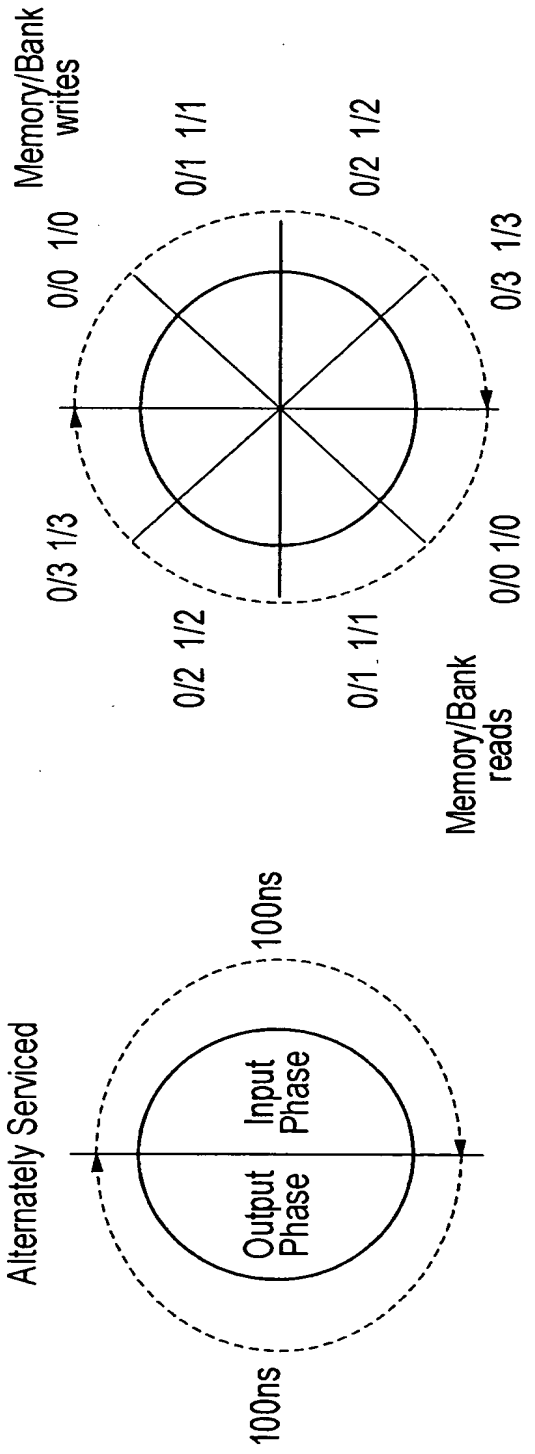

Packets
FIA Interface
Read Scheduler/ Output Processing
MDRR Module
Output Phase
Packet Memory
Input Phase
Input Processing Logic
Queue Manager
RED Module
Rx Interface
Incoming Packets
Data Flow
Control Flow

FIG. 14



200ns: 4 bursts of 4 write: 80ns, 4 bursts of 4 read: 80ns, turnaround: 40ns

FIG. 15

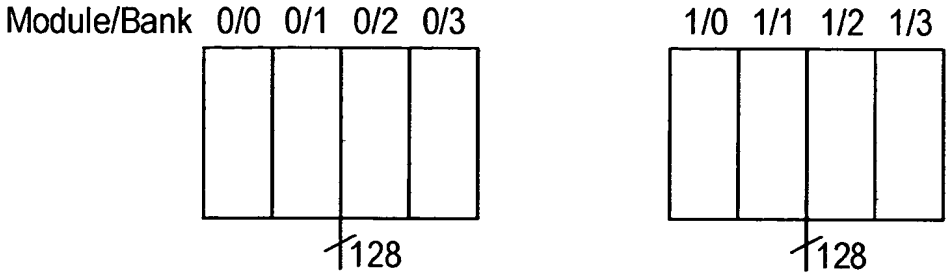


FIG. 16A

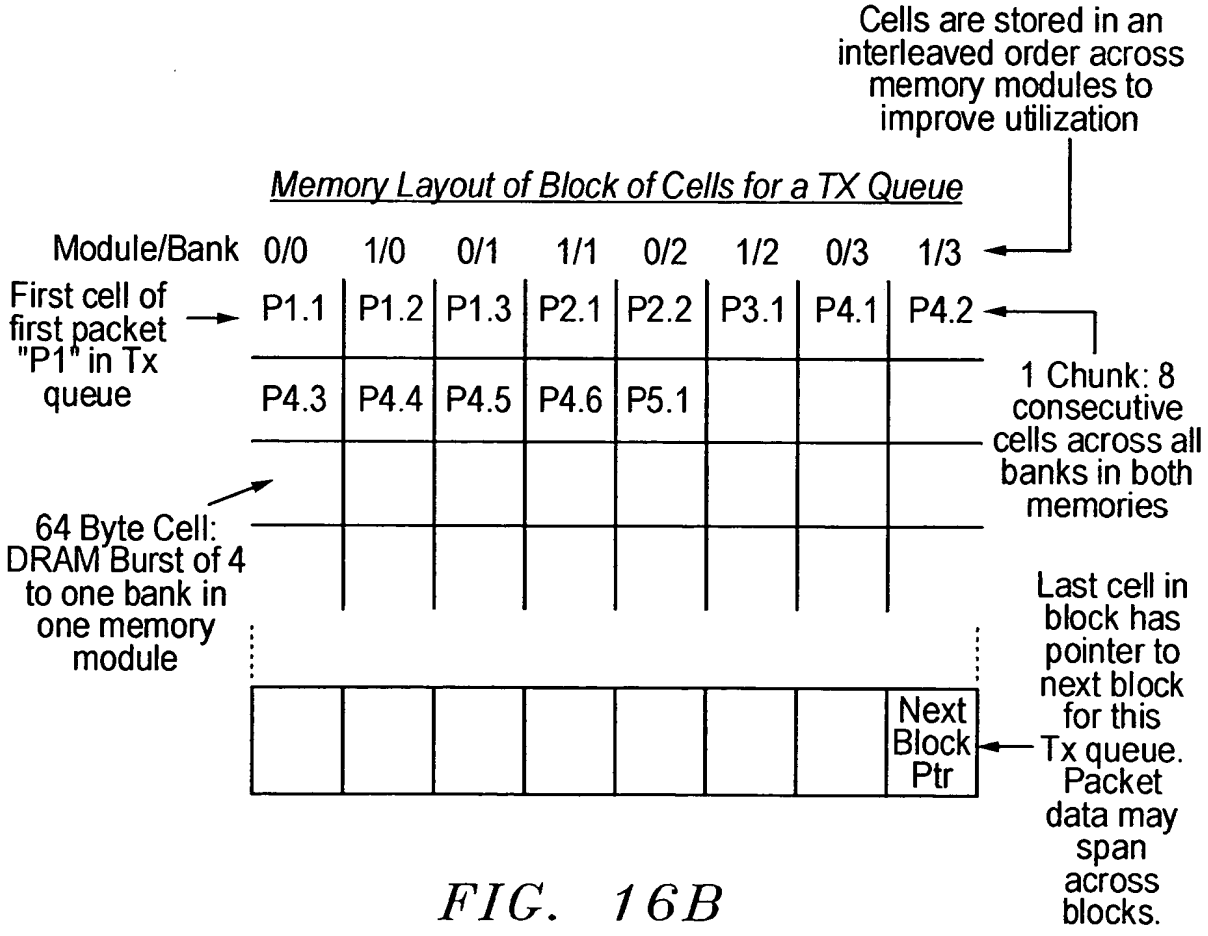


FIG. 16B

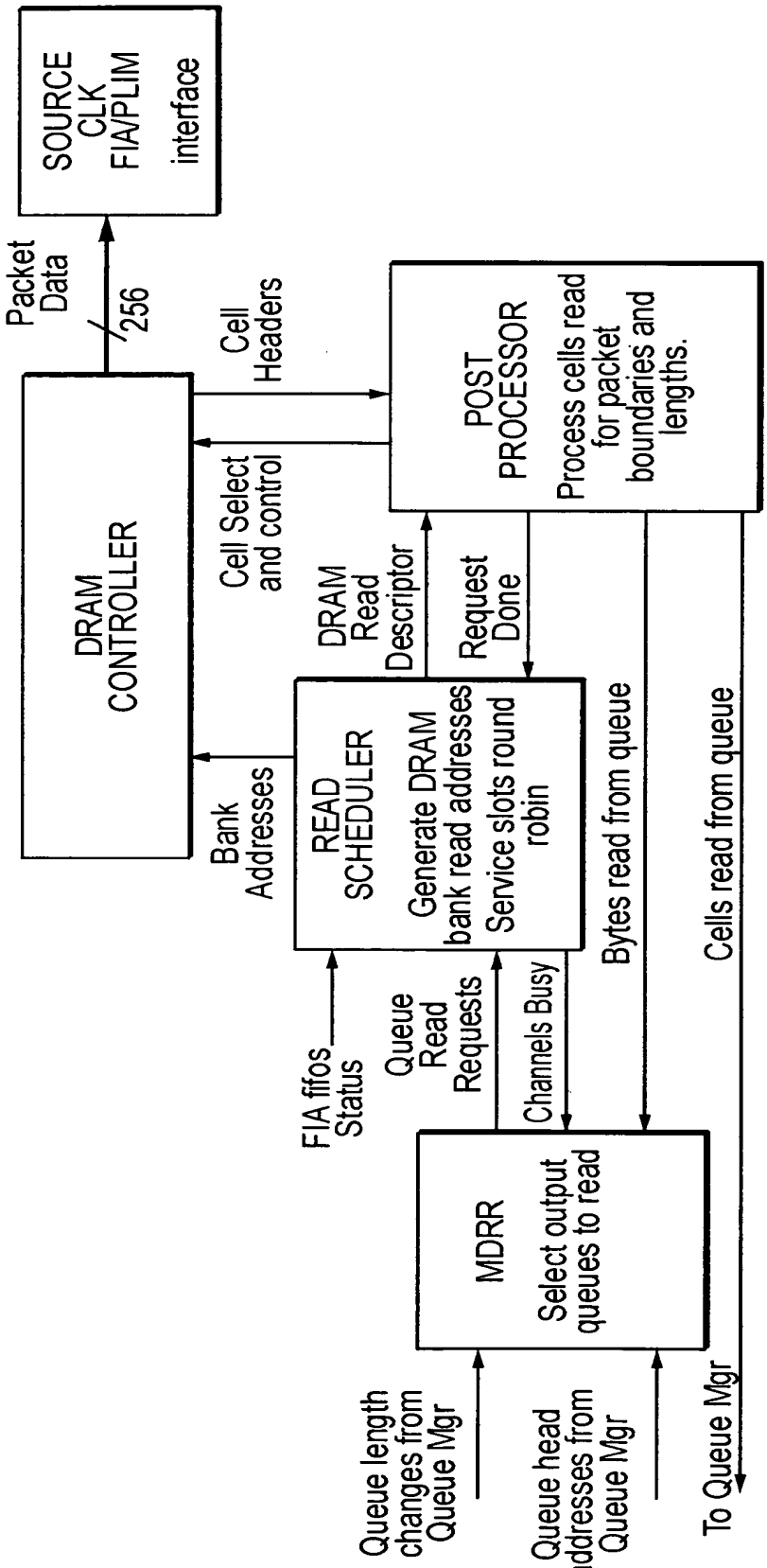

SOURCE CLK FIA/PLIM interface
Packet Data
256
DRAM CONTROLLER
Cell Headers
Cell Select and control
POST PROCESSOR
Process cells read for packet boundaries and lengths.
DRAM Read Descriptor
Request Done
Bank Addresses
READ SCHEDULER
Generate DRAM bank read addresses
Service slots round robin
FIA fifos Status
Queue Read Requests
Channels Busy
Bytes read from queue
Cells read from queue
MDRR
Select output queues to read
Queue length changes from Queue Mgr
Queue head addresses from Queue Mgr
To Queue Mgr

FIG. 17

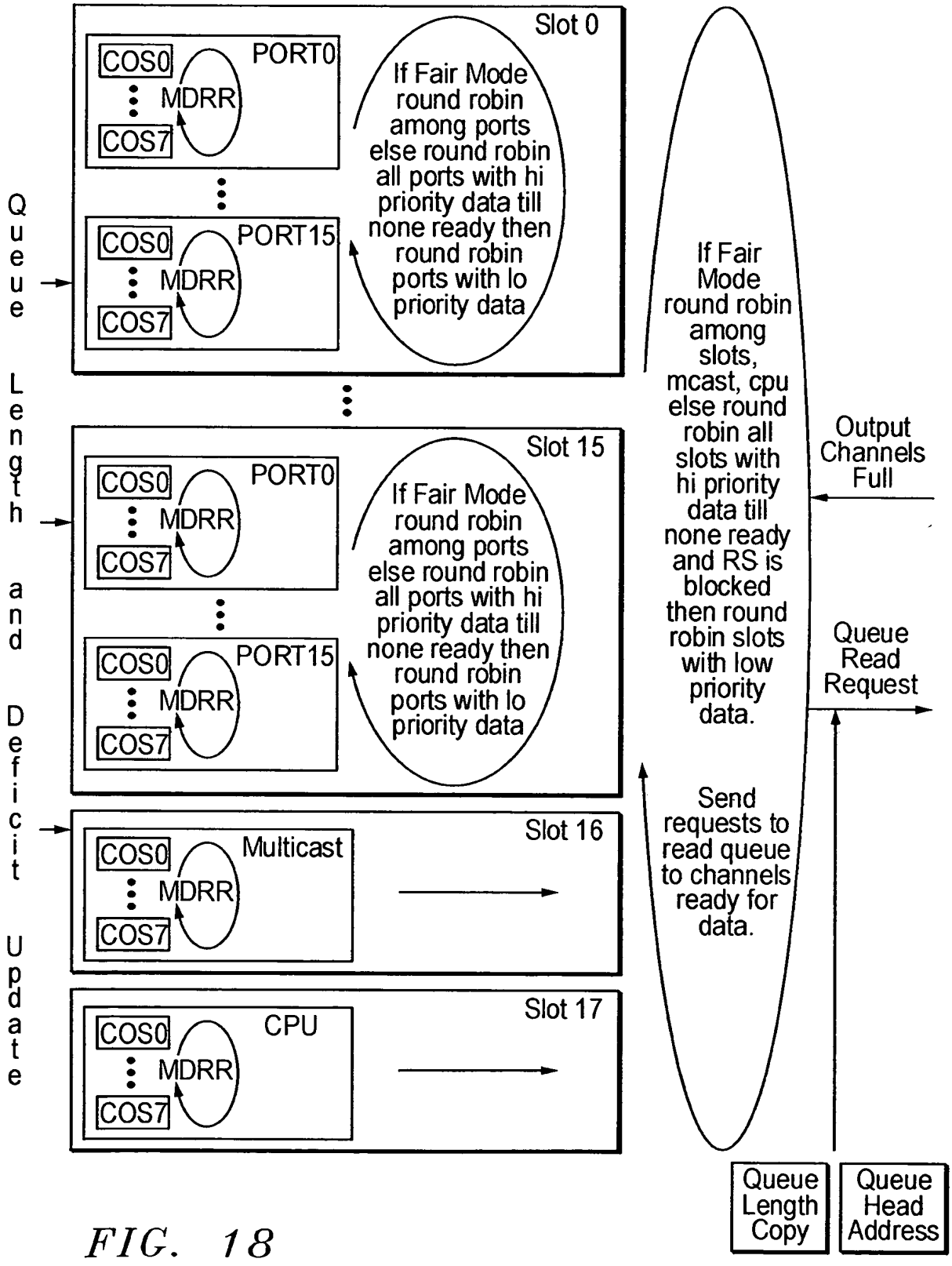

Slot 0
COS0
PORT0
MDRR
COS7
COS0
PORT15
MDRR
COS7
If Fair Mode round robin among ports else round robin all ports with hi priority data till none ready then round robin ports with lo priority data
Slot 15
COS0
PORT0
MDRR
COS7
COS0
PORT15
MDRR
COS7
If Fair Mode round robin among ports else round robin all ports with hi priority data till none ready then round robin ports with lo priority data
Slot 16
COS0
Multicast
MDRR
COS7
Slot 17
COS0
CPU
MDRR
COS7
Queue Length and Deficit Update
If Fair Mode round robin among slots, mcast, cpu else round robin all slots with hi priority data till none ready and RS is blocked then round robin slots with low priority data.
Output Channels Full
Queue Read Request
Send requests to read queue to channels ready for data.
Queue Length Copy
Queue Head Address

FIG. 18

FIG. 19

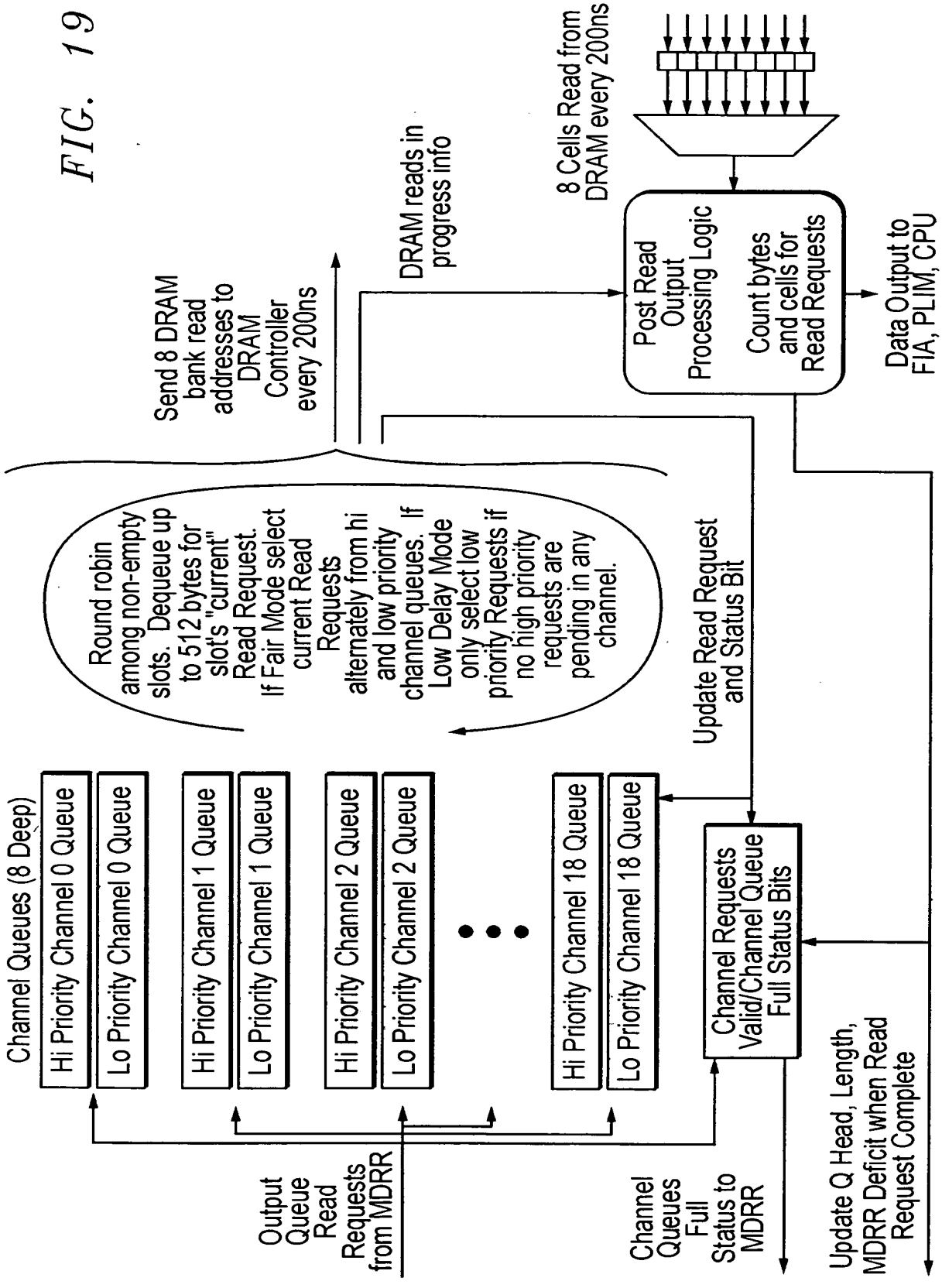
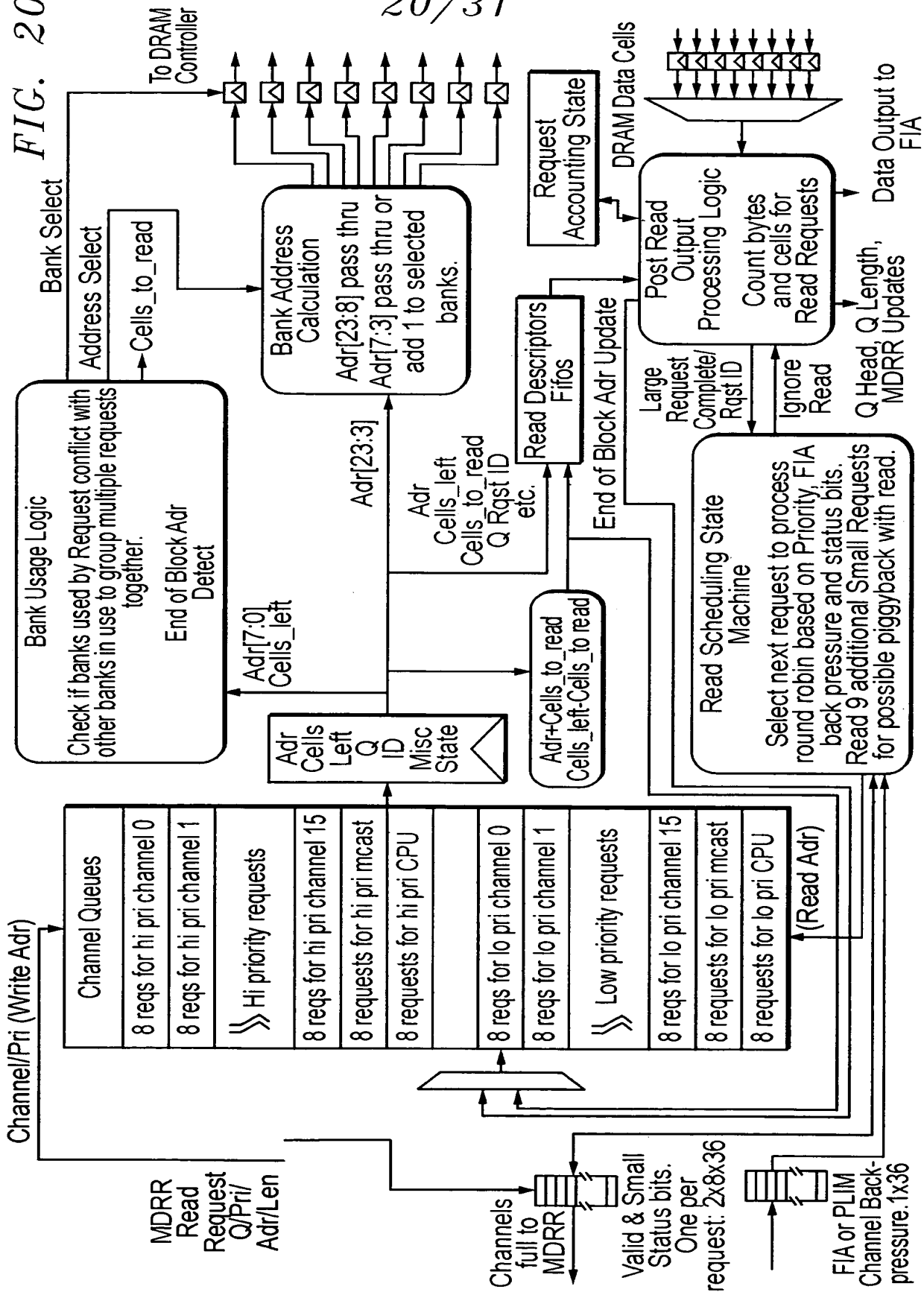

Send 8 DRAM bank read addresses to DRAM Controller every 200ns
DRAM reads in progress info
8 Cells Read from DRAM every 200ns
Post Read Output Processing Logic
Count bytes and cells for Read Requests
Data Output to FIA, PLIM, CPU
Round robin among non-empty slots. Dequeue up to 512 bytes for slot's "current" Read Request. If Fair Mode select current Read Requests alternately from hi and low priority channel queues. If Low Delay Mode only select low priority Requests if no high priority requests are pending in any channel.
Update Read Request and Status Bit
Channel Queues (8 Deep)
Hi Priority Channel 0 Queue
Lo Priority Channel 0 Queue
Hi Priority Channel 1 Queue
Lo Priority Channel 1 Queue
Hi Priority Channel 2 Queue
Lo Priority Channel 2 Queue
Hi Priority Channel 18 Queue
Lo Priority Channel 18 Queue
Channel Requests Valid/Channel Queue Full Status Bits
Output Queue Read Requests from MDRR
Channel Queues Full Status to MDRR
Update Q Head, Length, MDRR Deficit when Read Request Complete

FIG. 20


To DRAM Controller
Bank Select
Address Select
Cells_to_read
Bank Address Calculation
Adr[23:8] pass thru
Adr[7:3] pass thru or add 1 to selected banks.
Request Accounting State
DRAM Data Cells
Post Read Output Processing Logic
Count bytes and cells for Read Requests
Data Output to FIA
Bank Usage Logic
Check if banks used by Request conflict with other banks in use to group multiple requests together.
End of Block Adr Detect
Adr[23:3]
Adr
Cells_left
Cells_to_read
Q Rqst ID
etc.
Read Descriptors Fifos
End of Block Adr Update
Large Request Complete/ Rqst ID
Ignore Read
Q Head, Q Length, MDRR Updates
Adr[7:0]
Cells_left
Adr
Cells
Left
Q
ID
Misc
State
Adr+Cells_to_read
Cells_left-Cells_to_read
Read Scheduling State Machine
Select next request to process round robin based on Priority, FIA back pressure and status bits. Read 9 additional Small Requests for possible piggyback with read.
Channel/Pri (Write Adr)
Channel Queues
8 reqs for hi pri channel 0
8 reqs for hi pri channel 1
Hi priority requests
8 reqs for hi pri channel 15
8 requests for hi pri mcast
8 requests for hi pri CPU
8 reqs for lo pri channel 0
8 reqs for lo pri channel 1
Low priority requests
8 reqs for lo pri channel 15
8 requests for lo pri mcast
8 requests for lo pri CPU
(Read Adr)
MDRR Read Request Q/Pri/ Adr/Len
Channels full to MDRR
Valid & Small Status bits. One per request: 2x8x36
FIA or PLIM Channel Back-pressure. 1x36

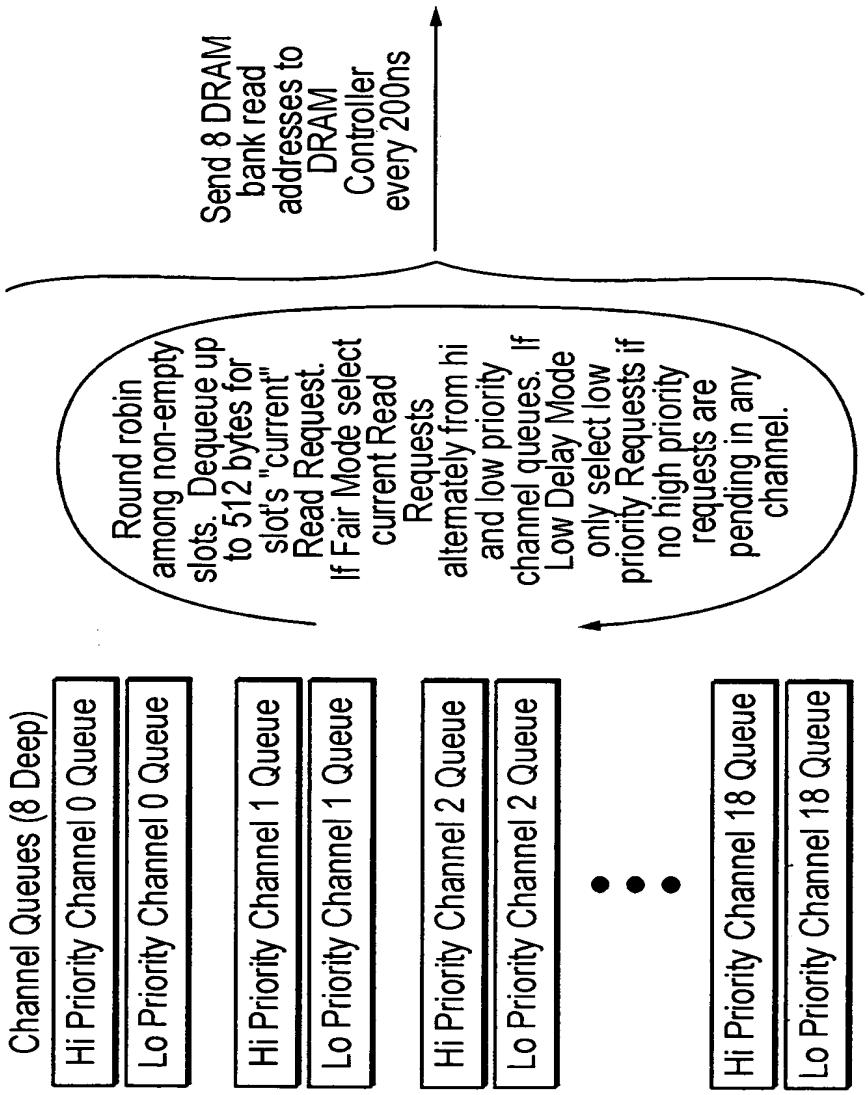

Channel Queues (8 Deep)
Hi Priority Channel 0 Queue
Lo Priority Channel 0 Queue
Hi Priority Channel 1 Queue
Lo Priority Channel 1 Queue
Hi Priority Channel 2 Queue
Lo Priority Channel 2 Queue
Hi Priority Channel 18 Queue
Lo Priority Channel 18 Queue
Round robin among non-empty slots. Dequeue up to 512 bytes for slot's "current" Read Request. If Fair Mode select current Read Requests alternately from hi and low priority channel queues. If Low Delay Mode only select low priority Requests if no high priority requests are pending in any channel.
Send 8 DRAM bank read addresses to DRAM Controller every 200ns

FIG. 21

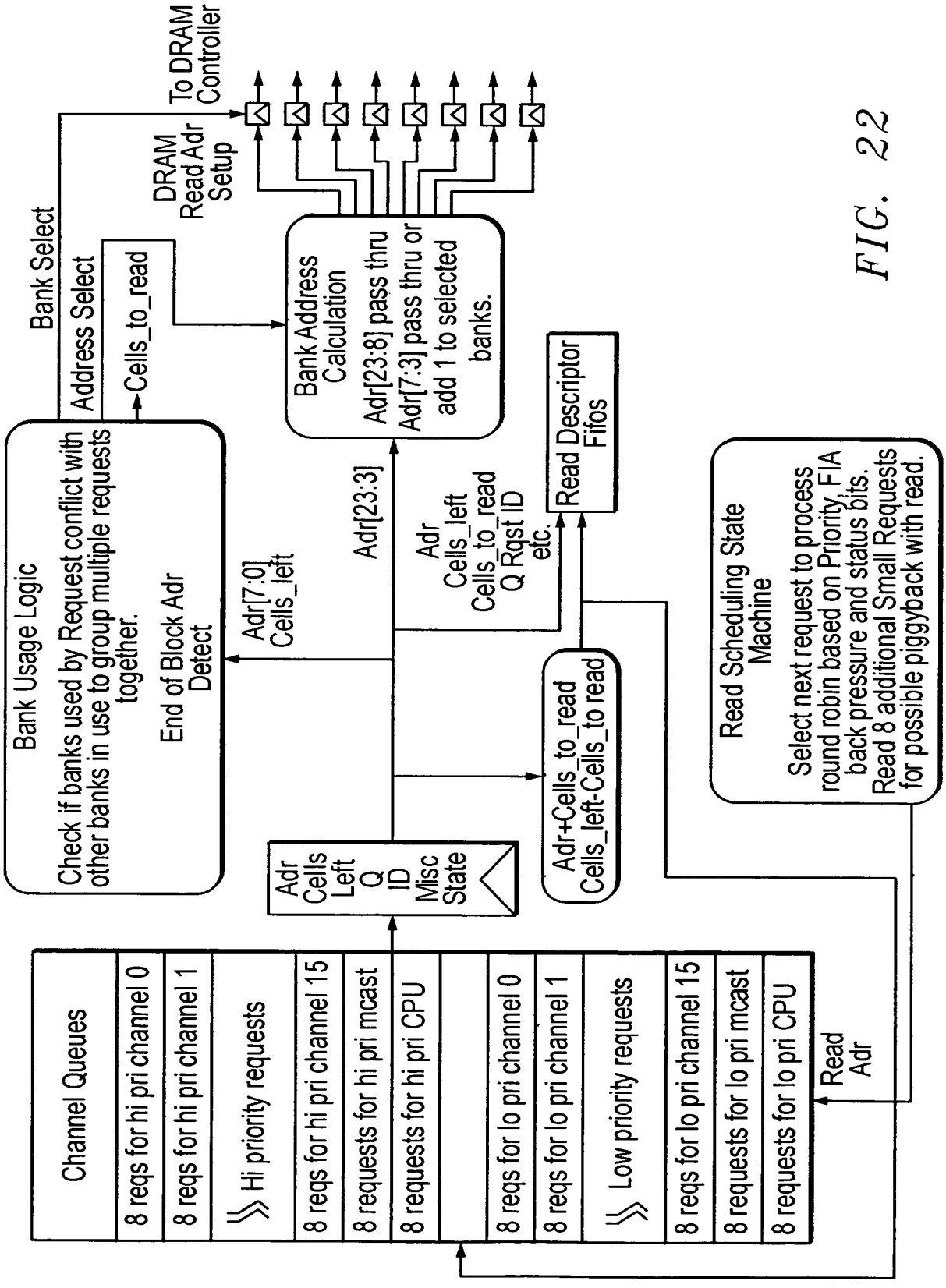

Channel Queues
8 reqs for hi pri channel 0
8 reqs for hi pri channel 1
Hi priority requests
8 reqs for hi pri channel 15
8 requests for hi pri mcast
8 requests for hi pri CPU
8 reqs for lo pri channel 0
8 reqs for lo pri channel 1
Low priority requests
8 reqs for lo pri channel 15
8 requests for lo pri mcast
8 requests for lo pri CPU
Read Adr
Adr Cells Left Q ID Misc State
Adr+Cells_to_read Cells_left-Cells_to_read
Read Scheduling State Machine
Select next request to process round robin based on Priority, FIA back pressure and status bits. Read 8 additional Small Requests for possible piggyback with read.
Bank Usage Logic
Check if banks used by Request conflict with other banks in use to group multiple requests together.
End of Block Adr Detect
Adr[7:0] Cells_left
Adr[23:3]
Adr Cells_left Cells_to_read Q Rqst ID etc.
Read Descriptor Fifos
Bank Address Calculation
Adr[23:8] pass thru
Adr[7:3] pass thru or add 1 to selected banks.
Cells_to_read
Address Select
Bank Select
DRAM Read Adr Setup
To DRAM Controller

FIG. 22

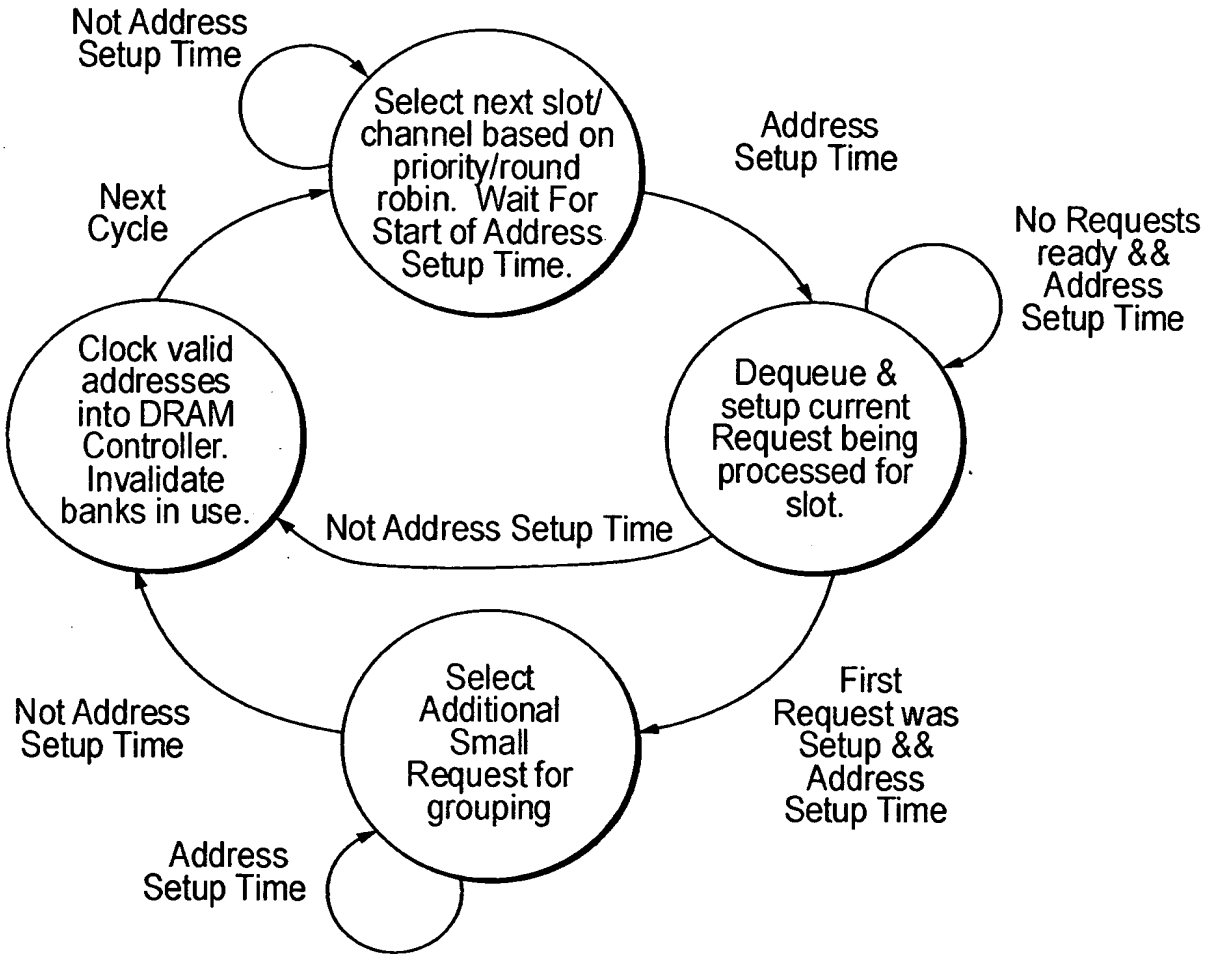

Not Address Setup Time
Select next slot/ channel based on priority/round robin. Wait For Start of Address Setup Time.
Address Setup Time
No Requests ready && Address Setup Time
Next Cycle
Clock valid addresses into DRAM Controller. Invalidate banks in use.
Dequeue & setup current Request being processed for slot.
Not Address Setup Time
Select Additional Small Request for grouping
First Request was Setup && Address Setup Time
Not Address Setup Time
Address Setup Time

FIG. 23

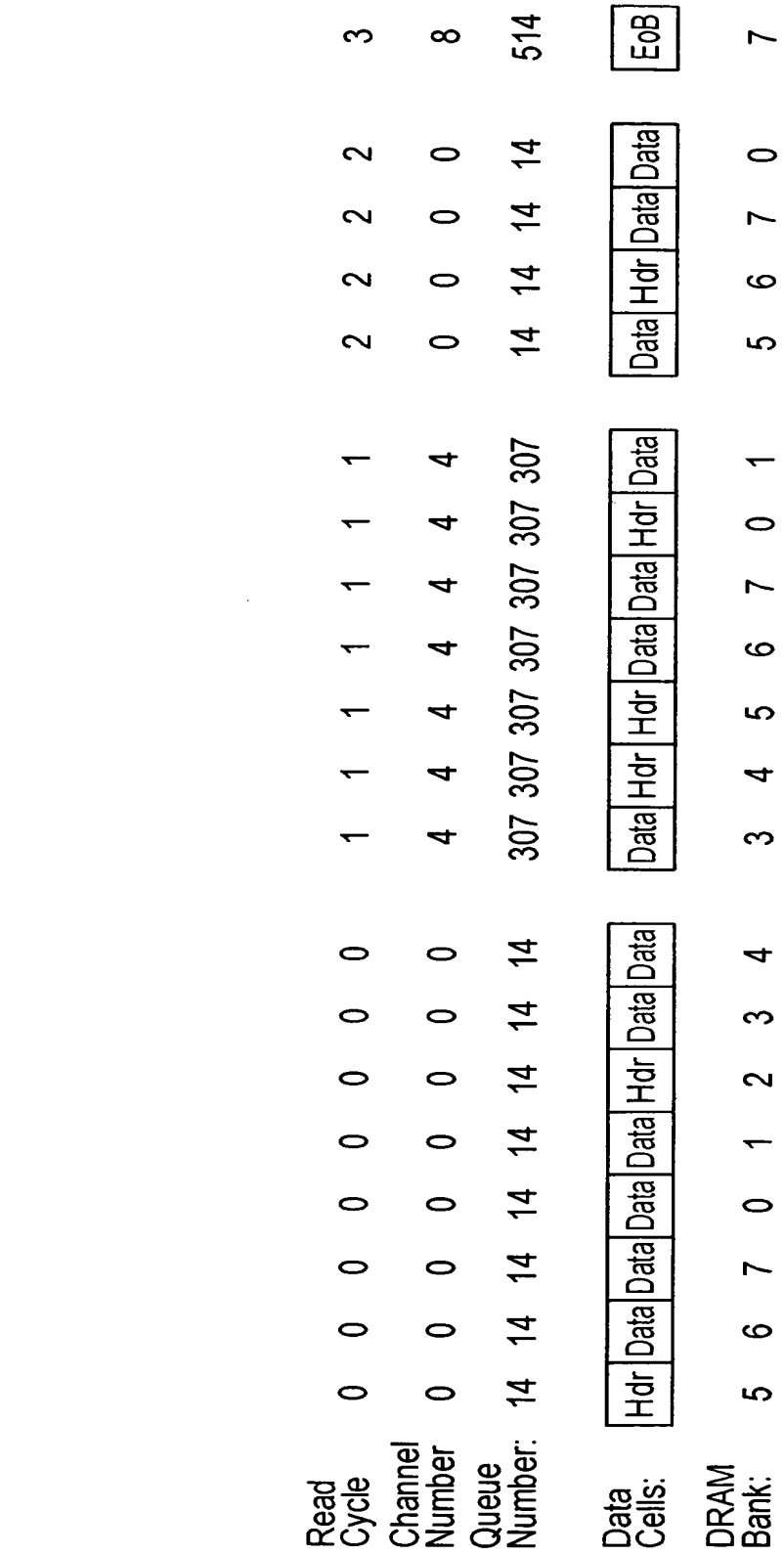

Read Cycle
Channel Number
Queue Number:
Data Cells:
DRAM Bank:
Hdr
Data
EoB

FIG. 24

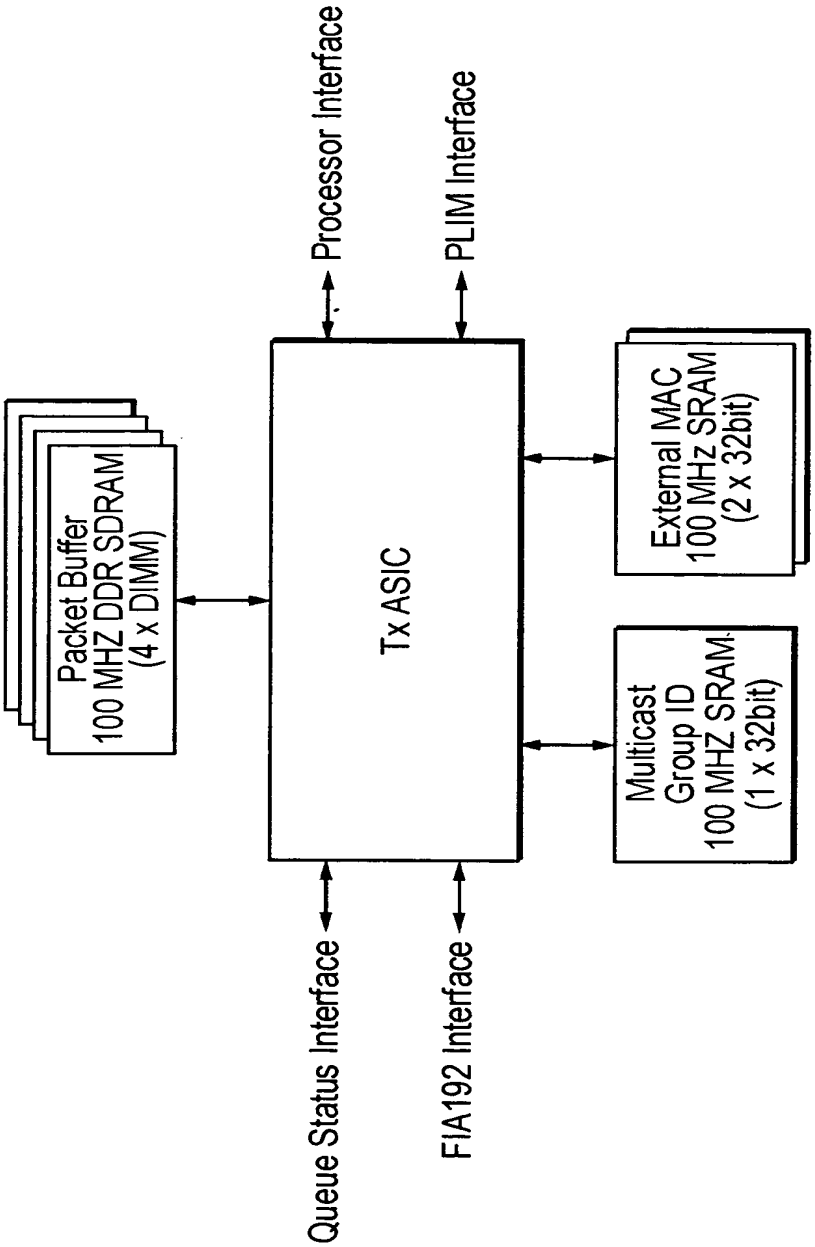

Processor Interface
PLIM Interface
Packet Buffer
100 MHZ DDR SDRAM
(4 x DIMM)
Tx ASIC
External MAC
100 MHz SRAM
(2 x 32bit)
Multicast
Group ID
100 MHZ SRAM
(1 x 32bit)
Queue Status Interface
FIA192 Interface

FIG. 25

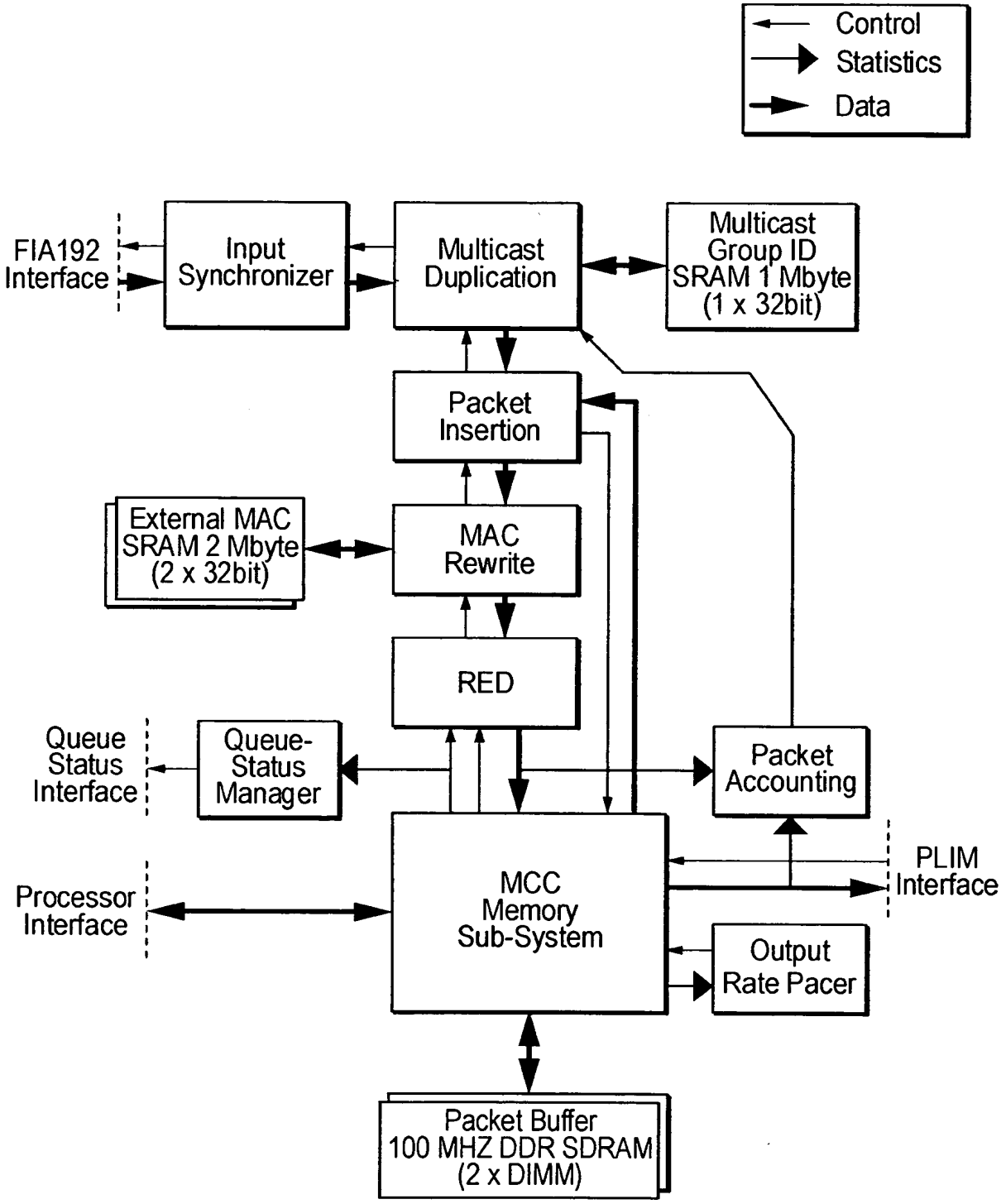

Control
Statistics
Data
FIA192 Interface
Input Synchronizer
Multicast Duplication
Multicast Group ID SRAM 1 Mbyte (1 x 32bit)
Packet Insertion
External MAC SRAM 2 Mbyte (2 x 32bit)
MAC Rewrite
RED
Queue Status Interface
Queue-Status Manager
Packet Accounting
PLIM Interface
Processor Interface
MCC Memory Sub-System
Output Rate Pacer
Packet Buffer 100 MHZ DDR SDRAM (2 x DIMM)

FIG. 26

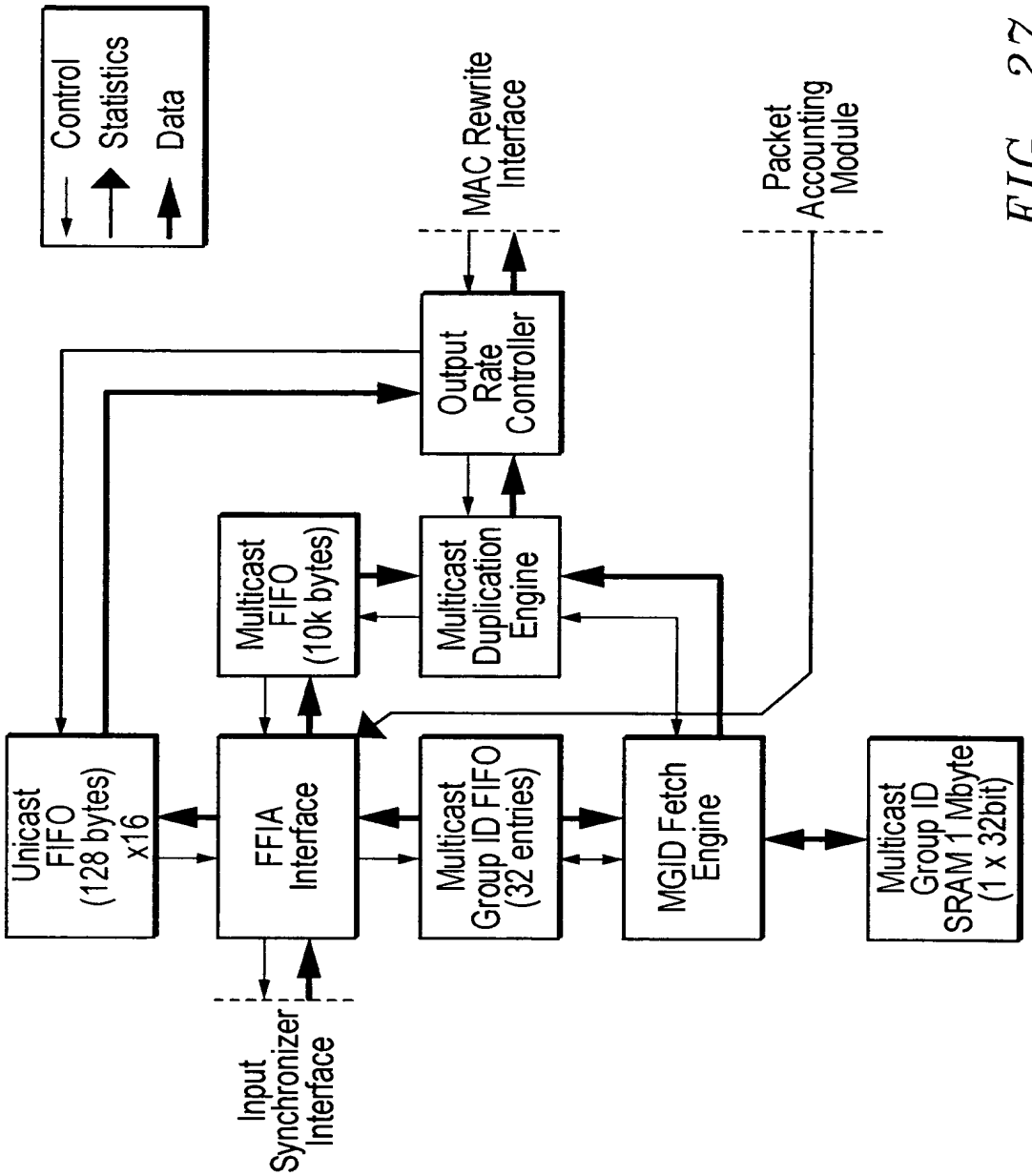

Control
Statistics
Data
MAC Rewrite Interface
Packet Accounting Module
Output Rate Controller
Multicast FIFO (10k bytes)
Multicast Duplication Engine
Unicast FIFO (128 bytes) x16
FFIA Interface
Multicast Group ID FIFO (32 entries)
MGID Fetch Engine
Multicast Group ID SRAM 1 Mbyte (1 x 32bit)
Input Synchronizer Interface

FIG. 27

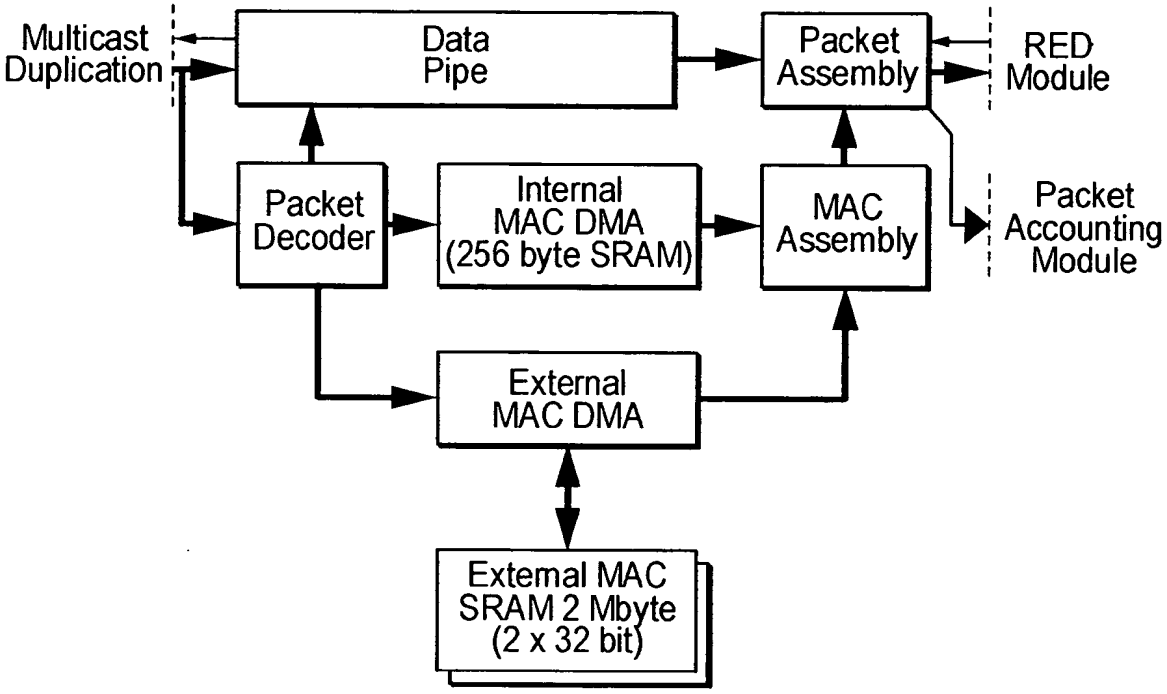

Multicast Duplication
Data Pipe
Packet Assembly
RED Module
Packet Decoder
Internal MAC DMA (256 byte SRAM)
MAC Assembly
Packet Accounting Module
External MAC DMA
External MAC SRAM 2 Mbyte (2 x 32 bit)

FIG. 28

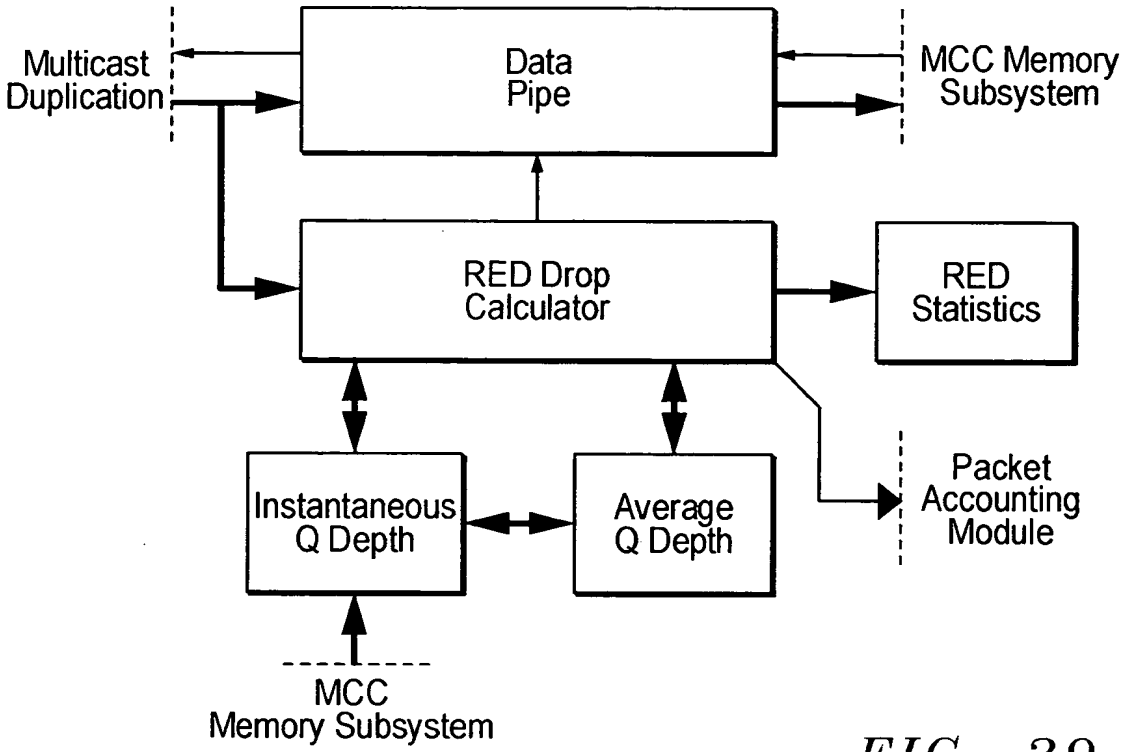

Multicast Duplication
Data Pipe
MCC Memory Subsystem
RED Drop Calculator
RED Statistics
Instantaneous Q Depth
Average Q Depth
Packet Accounting Module
MCC Memory Subsystem

FIG. 29

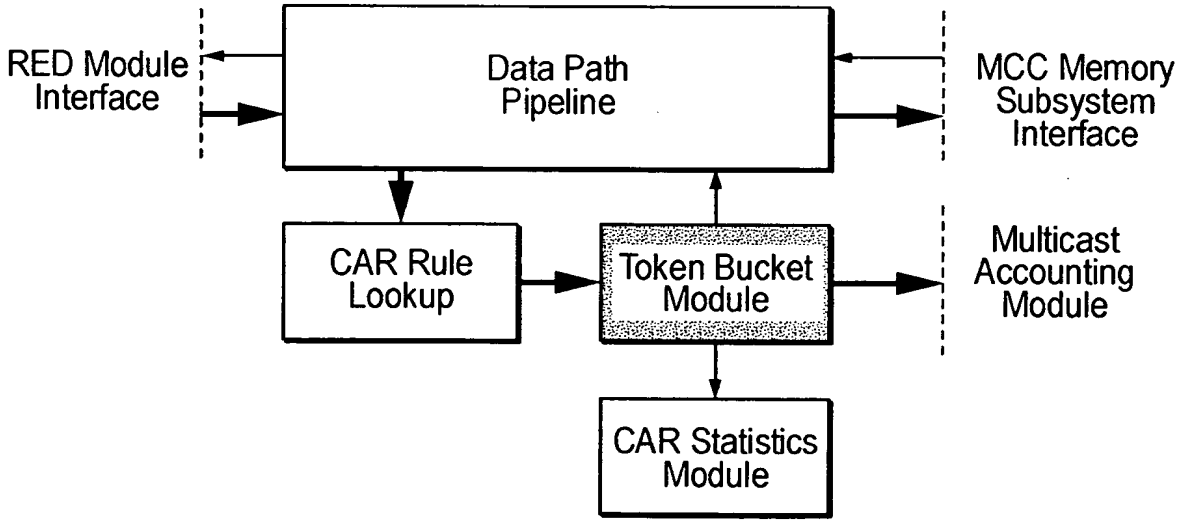

RED Module Interface
Data Path Pipeline
MCC Memory Subsystem Interface
CAR Rule Lookup
Token Bucket Module
Multicast Accounting Module
CAR Statistics Module

FIG. 30

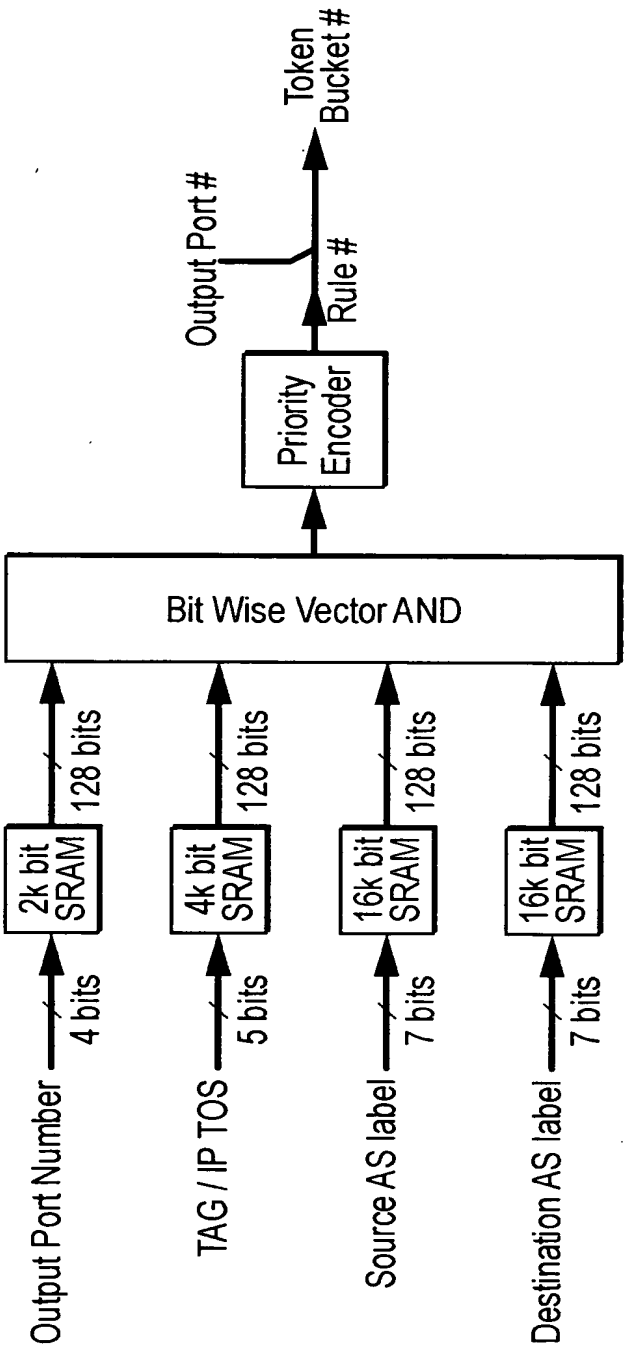

Output Port Number
4 bits
TAG / IP TOS
5 bits
Source AS label
7 bits
Destination AS label
7 bits
2k bit SRAM
4k bit SRAM
16k bit SRAM
16k bit SRAM
128 bits
128 bits
128 bits
128 bits
Bit Wise Vector AND
Priority Encoder
Output Port #
Rule #
Token Bucket #

FIG. 31

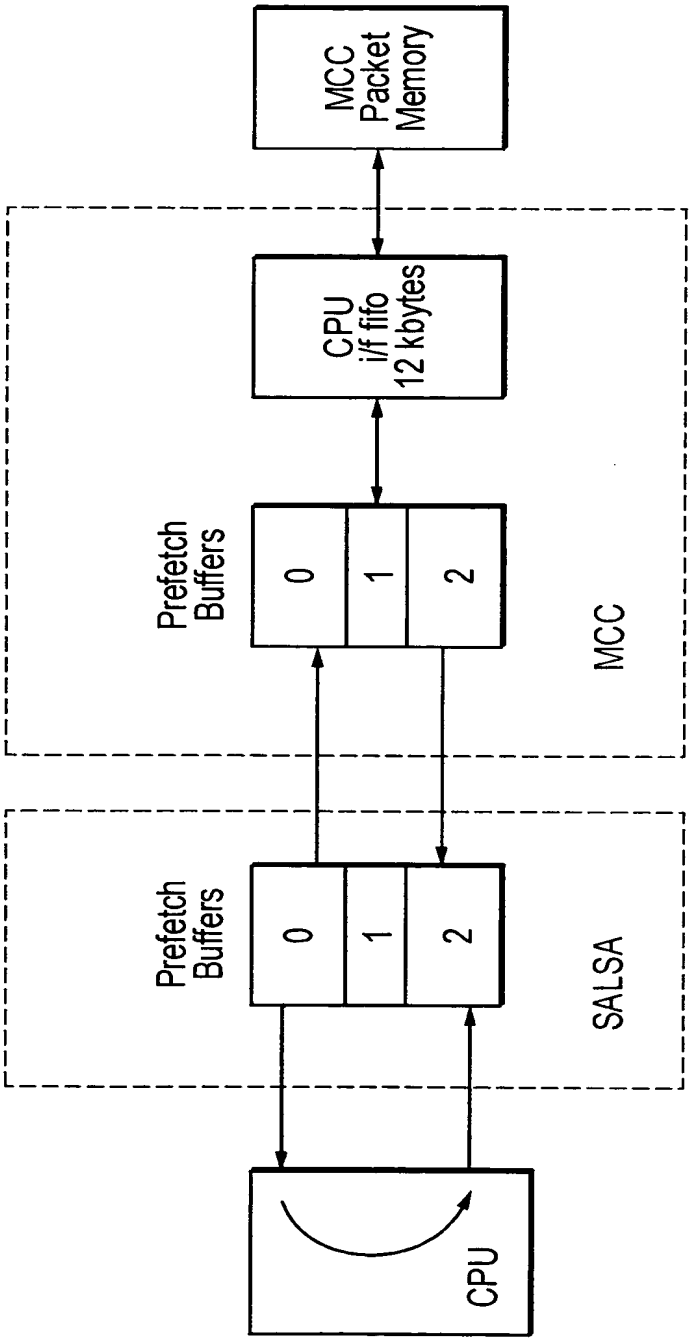

MCC Packet Memory
CPU i/f fifo 12 kbytes
Prefetch Buffers
0
1
2
MCC
Prefetch Buffers
0
1
2
SALSA
CPU

FIG. 32